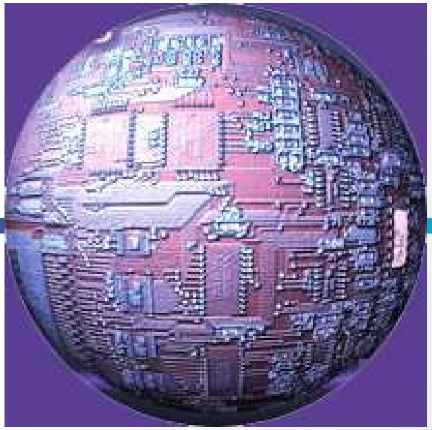


Printed Circuit Board manufacturing

PCB (Printed Circuit Board), NYÁK
PWB (Printed Wiring Board), NYHL

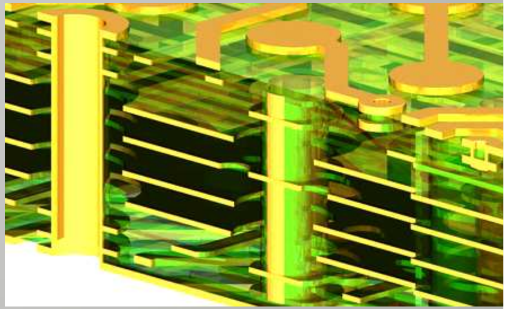
Wire network + mechanical support + base of assembly

Benefits:

- Higher load, better dissipation, better surface/cross section ratio
- **Automatic assembly, control, and rework**
- Better reliability

PCB types

- Laminates (substrates): rigid - flex
- Number of layers:
  - *Single layer*
  - *Double layers, through-hole plated,*
  - *Multilayer (2 – 20 + layers)*



- Feature size: width of conductiv and insulating stripes
  - *normal: 0,4 – 0,6 mm >16mil*
  - *Fine : 0,3 – 0,4 mm ~12 – 16 mil*
  - *Very fine: 0,1 – 0,2 mm ~ 4 – 8 mil*

(1 raster = 2,54mm, 1 mil = 0,01raster)

Subtraktiv, additiv, semi-additiv

Main steps of manufacturing

- Materials selection **(laminate, copper foil)**
- Mechanical forming **(drilling, cutting)**
- Making hole conductive
- Galvanic plating
- Patterning
    - **Photolithography, screen printing**
    - **Etching**
- Solder mask
- Surface finishing: **metal plating (galvanic, immersion and electroless)**

Laminate materials and types

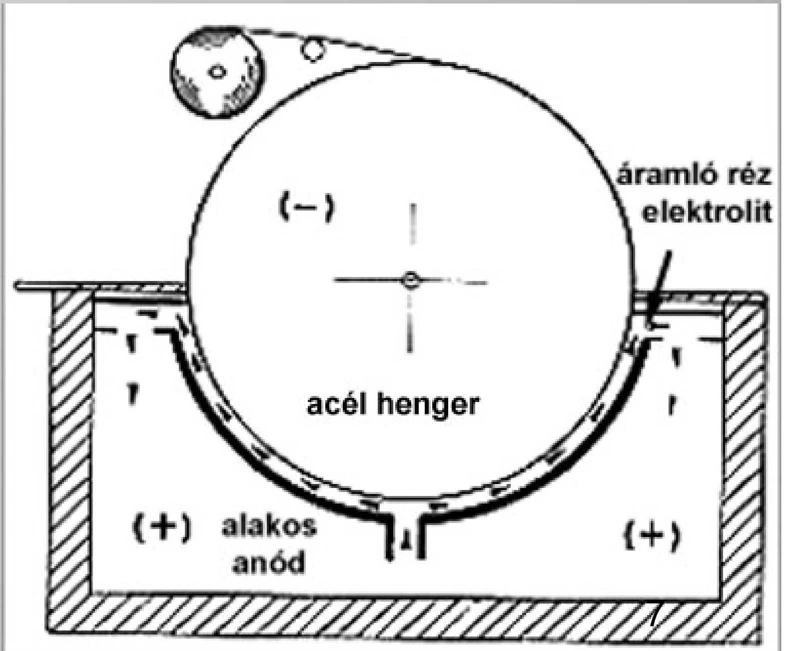
FR series (flame retardant)

- FR-2: paper reinforced phenolic
  - Dark yellow, stable size
- FR-3: paper reinforced epoxy
  - Light beige, good electrical properties, suitable for hole plating
- FR-4: wowen glass reinforced epoxi
  - Transparent yellwish-green, good machinable, plateable, minimal water absorption
- FR-5: similar to FR-4, better heat resistance, higher T_g
- CEM 1: paper and glass reinforced epoxy: cheaper
- CEM 3: wowen and non-wowen glass reinforced epoxy

Properties	FR-3	FR-4	FR-5
R_{bulk}, Ωcm (40°C)	$4\ 10^{12}$	8.10^{14}	8.10^{14}
$R_{\square}$, Ω (40°C)	$4\ 10^{12}$	$3\ 10^{12}$	$3\ 10^{15}$
ε_{rel}, (1 MHz)	4,9	4,7	4,6
tgδ (1 MHz) (GHz)	0,04	0,02	0,015
Tolerance of the solder baath (sec)	25	>120	>120
Water absorption (mg)	na	15	na
Tg, glass transition temperature		150	>165
Thermal expansion coefficient (z axis %) 25-275°C		5.5	

Copper foil

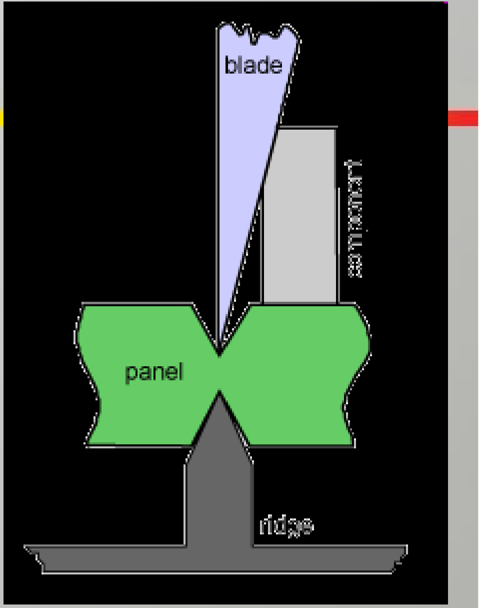
- Thickness: 17,5μm, 35μm, (70μm, 105μm)
  - Semi-additiv: 5μm Cu + protectiv coating
  - special (eg. Car electronic 400 μm)
- Manufacturing: galvanoplastic
  - Electroplating to a rotate steel cilinder, detach after half round
- Mounting:
  - Adhesiv foil or a dissolved thermosetting resin



Preparations of the laminates

- Cutting
- Drilling
- Degreasing
- Micro-etching and dissolve the oxid layer

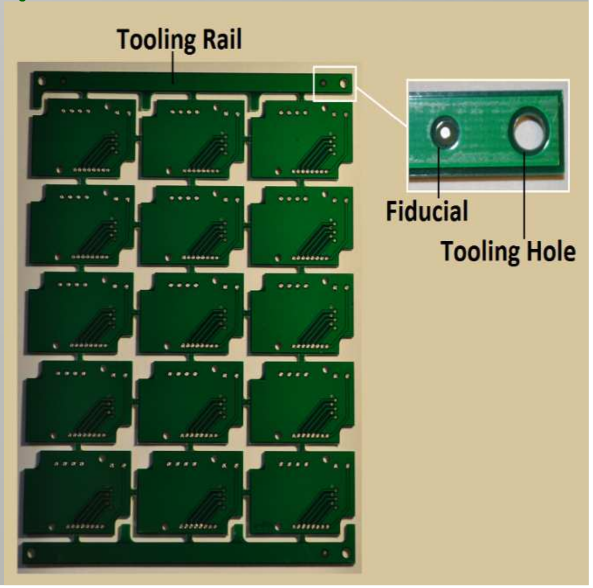
Mechanical processes



- *Cutting:* usual panel size is 500 – 800mm
  Free border (tooling rail)
  Back end: routing
- *Drilling:* single side: end of line, not critical

  Double side, multilayer: key process, one of the first steps. Need a smooth inner surface for metallization

  Aspect ratio: hole length/hole diameter: less than 7 - 10



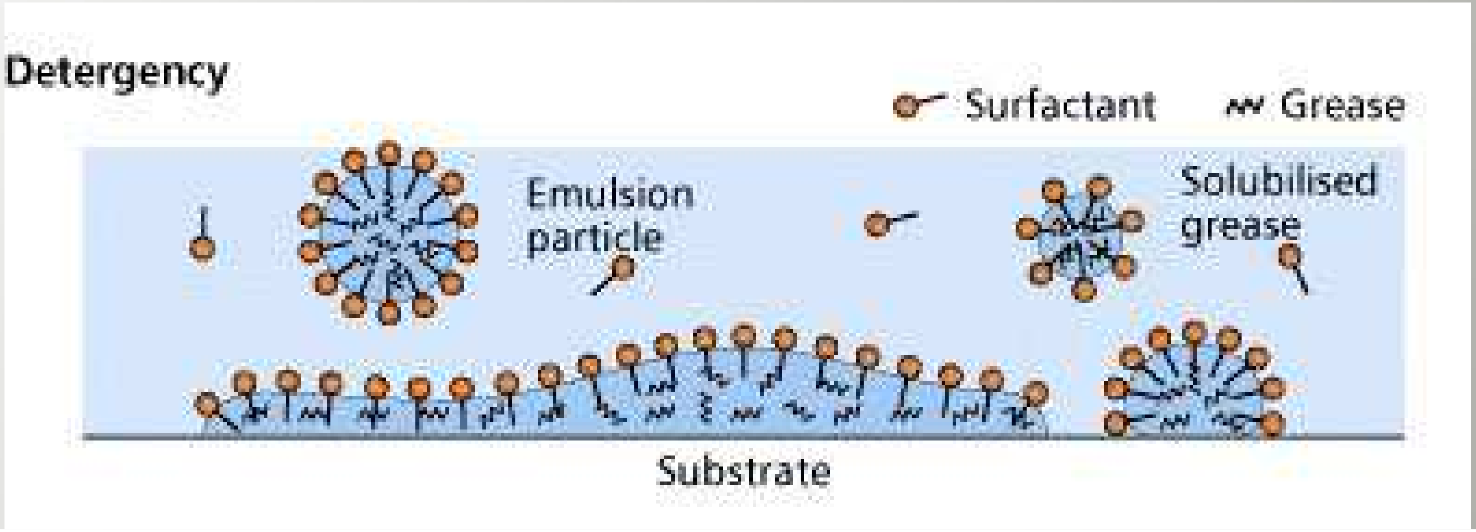
Drill tools

- **Material: Tungsten-carbide**
- **(Slope): 30 – 40^{o}**
- **(Top angle): ~140^{o}**
- **Speed (rev):**
  10-90000/min
  smaller diameter, higher speed
- **Min. d =0,2 – 0,15 mm**

Suface cleaning

- **Mechanical: abrasive cylinder, pumice, (wet)**
- **Degreasing: goal is the uniform adhesion of the new coatings (photoresists, masks, metals)**
  - **Water base materials:**
    - *Alkaline: NaOH,* Na_2CO_3, Na_3PO_4
    - *Detegents, surfactans*

Dip or spray methods



Removing oxide layer

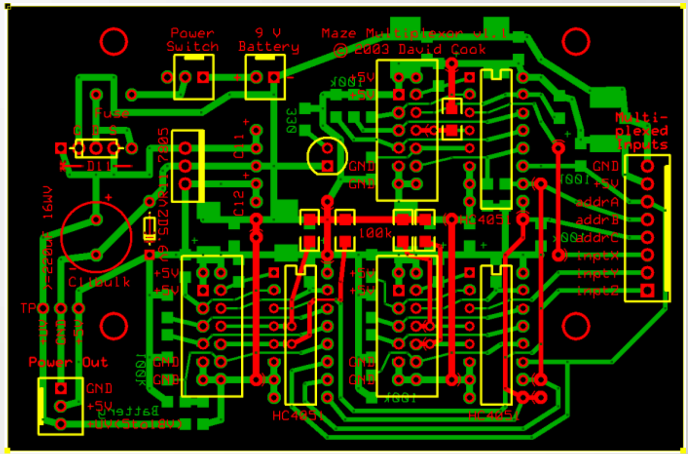
- **Oxidized surface contains:** Cu_2O, $Cu(OH)_2 \cdot CuCO_3$,
- **Decrease adhesion of the new films eg. photoresist, metal**
- **Usually acid solvents: sulfuric or hydrochloride acids (10 – 20 % w/w)**
- **Curing time: 0,5 - 1 min at room temperature**

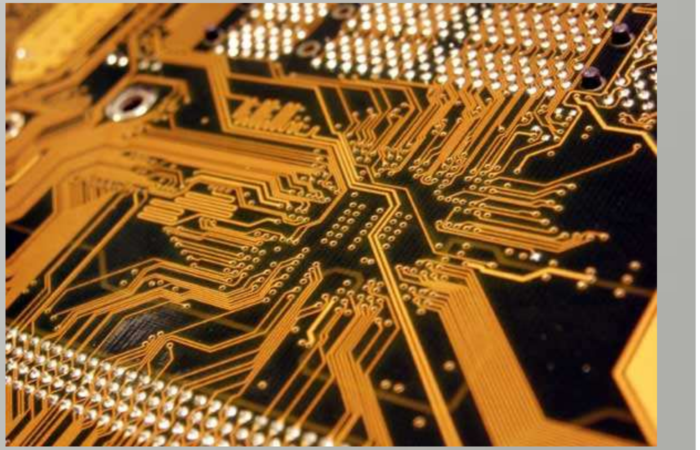
Printed Circuit Imaging

Photomask

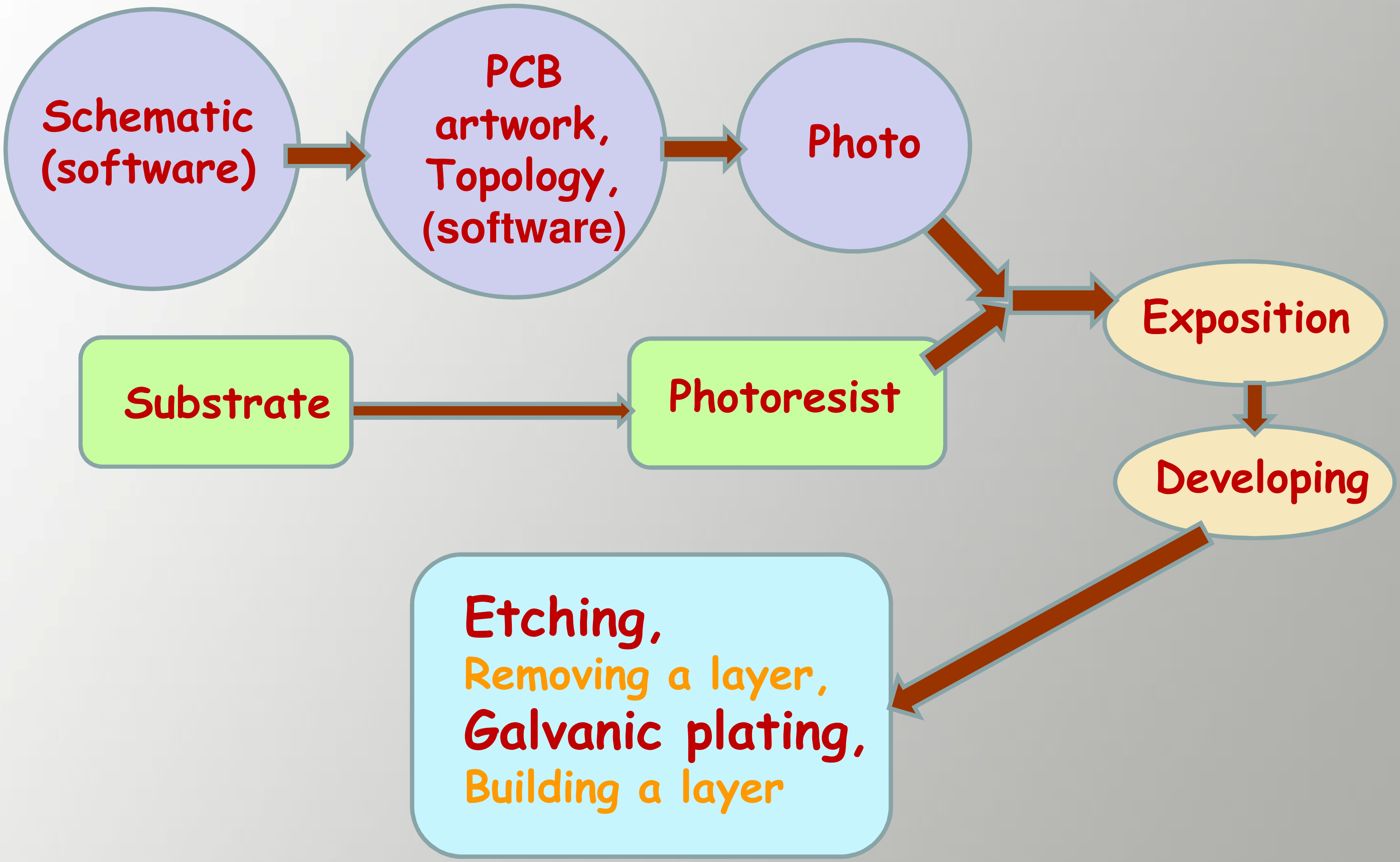
Photolithography

Sreen printing





Realization of drawing
Main steps of the phtolithography



Schematic (software)

PCB artwork, Topology, (software)

Photo

Substrate

Photoresist

Exposition

Developing

Etching,
Removing a layer,
Galvanic plating,
Building a layer

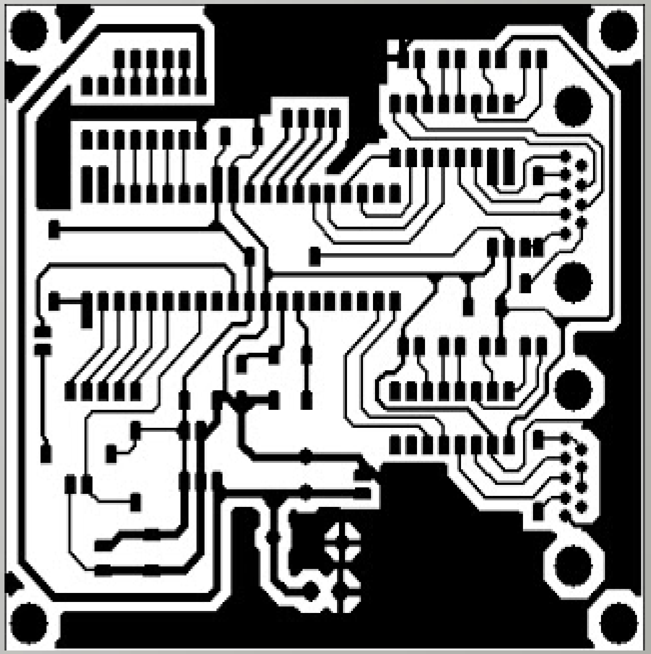
Photomask preparation

Its role: transfer the pattern

Master artwork: the first, original drawing, the copies are the technological photos

- **Manual methods: tint drawing, peelable patterns (chartpack, alfaset) → contact photo**
- **Computer aided methods:**
  - **Circuit design programs**
  - **PCB design programs:**

include: artworks (all layers), holes, soldermasks, final control (test) driver software



Gerber file:

- *x;y coordinates*
- *Light on/off*
- *aperture size*

Laser photoplotter

- Matrix printer system
- Plotter system
- Very high resolution
  8-10-16000 dpi

Masking methods

Goal: protect certain areas of the surface agains some physical or chemical attact

- In contact masks
- Out of contact, eg: screen mask

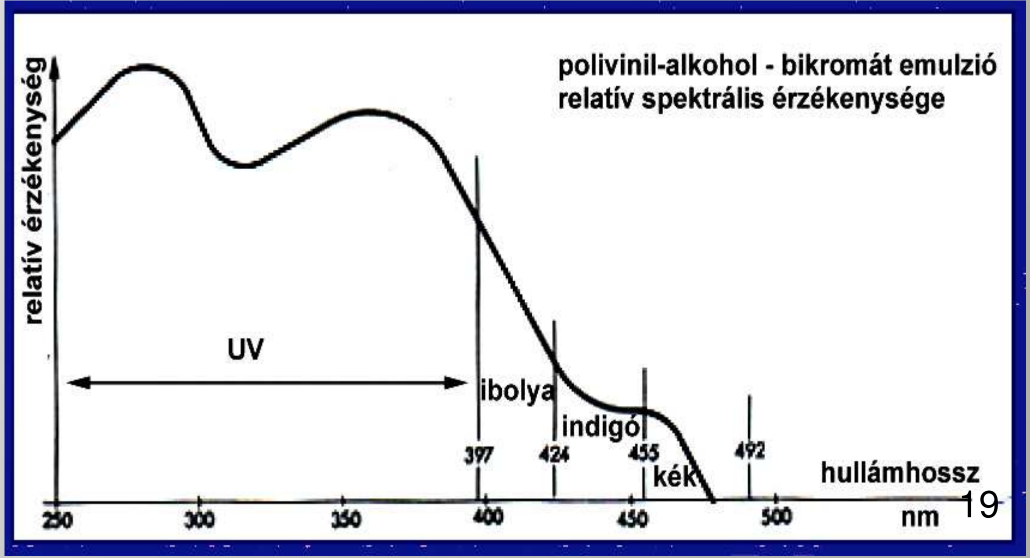
Masking methods 1. Photolithography

- Photoresist, photoimaigeable materials
- polimer layer
- Usable in PCB, hybrid IC and semiconductor industry
- Resolution, ~ minimal line width → 20 nm
- types:
  - positive negative
  - liquid solid (film)

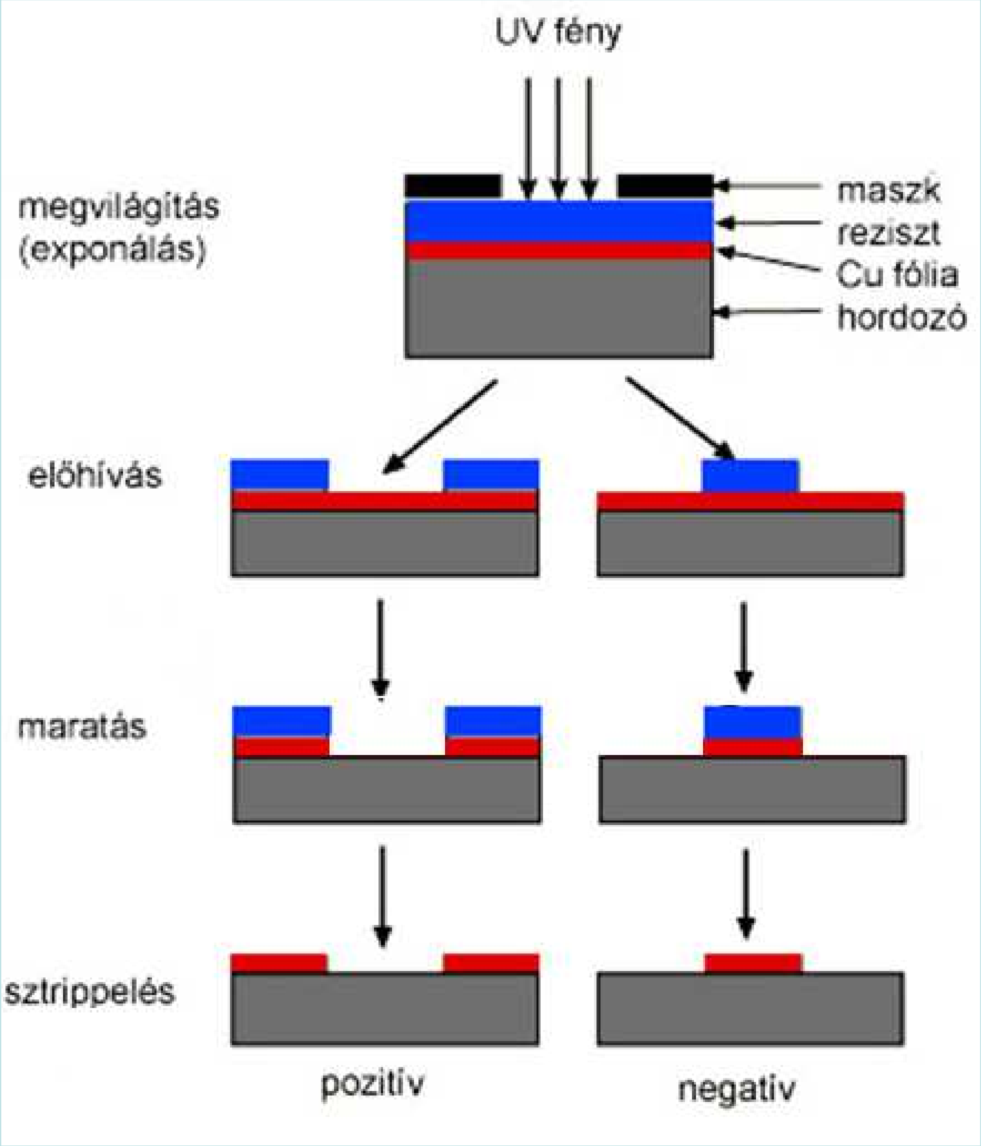
Photochemical background

- The absorbed photon give the energy quantum to the reaction (bonding or activation energy).
- $W = hc/\lambda \quad \Rightarrow$ to the successful reaction need a given energy (λ is lower than a given value).

h: Planck konstant
c: speed of light
λ: wavelenght



Types of photoresists



Positive: Depolimerisation caused by exposition, the molecular weight decreased, the solubility increased.

Negative: polimerisation, cross-linked bonds formation influence of light. The photoresist get nearly insoluble.

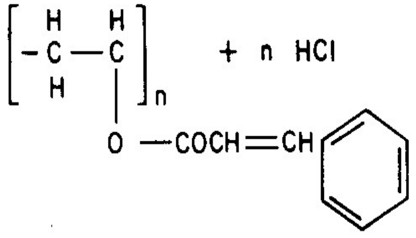
Liquid
Solid

Positive resists

- Sensitive for UV, but hardly for visible light
- Exposition: UV
- Developer: diluted NaOH (5 – 7 g/l)
- Stripper: organic solvent
- Avoid overdeveloping

Negative resists

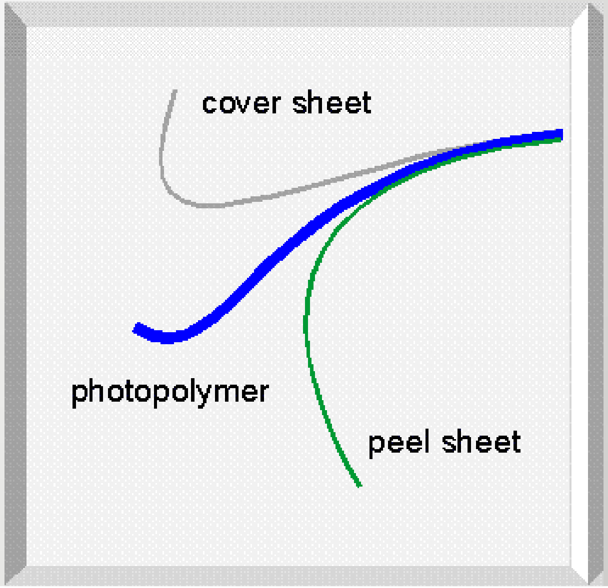
- Sensitive for light under 540 nm (yellow light needs in the workplace!)
- Exposition: UV
- Developer: weak alkaline solvent (1 – 2% Na_2CO_3)
- Stripper: stronger alkaline solvent (5% NaOH)
- Not sensitive to overdeveloping

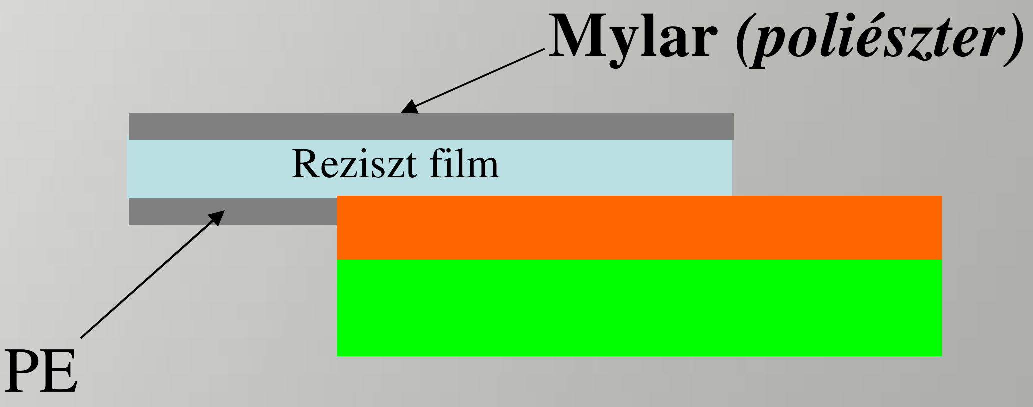


Polyvinyl cinnamate
(Photosensitive)

Solid resists

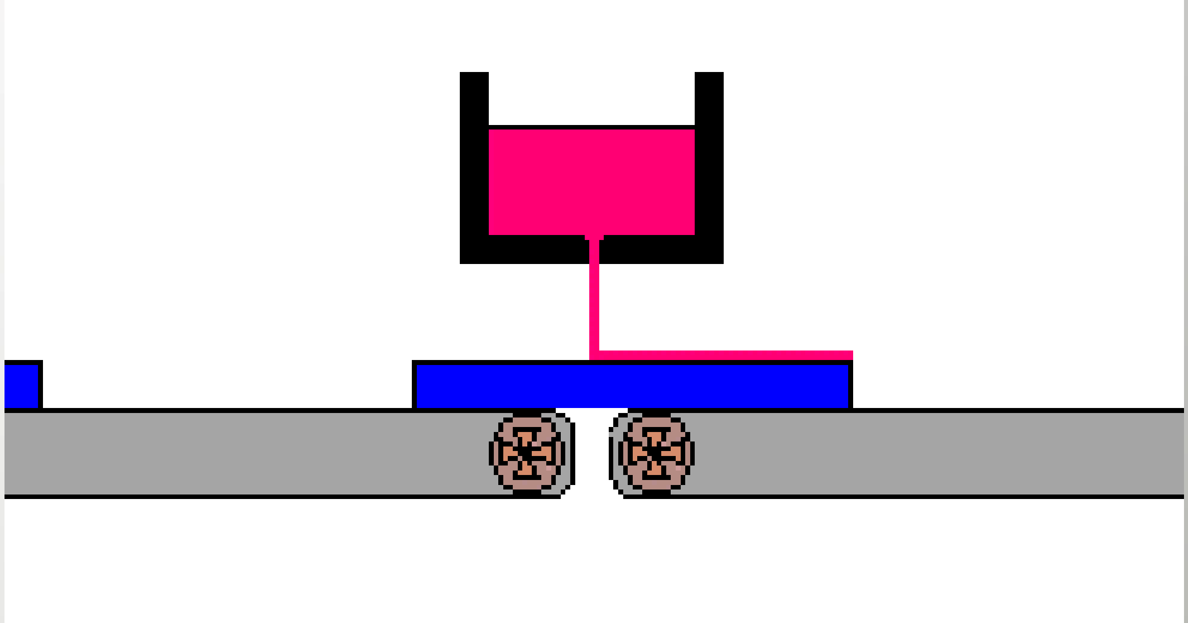
- „+” , „-”   the negative is more frequently used
- Thicker → important at the galvanisation
- Fewer manufacturing steps
- Uniform layer thickness





Manufacturing steps
(liquid resists)

1. Clear, degreased surface
2. Coating methods:
    - Spin coating ($d \sim v_k \sim r$)
    - Screen printing
    - Liquid carpet
3. Drying - 60…80°C
    - The solvent is volatilized
    - Film formation



Manufacturing steps 2

4. Exposition
   - Emulsion side stacked to the resist
   - UV - high-pressure Hg-vapor lamp (365nm)
   - -distance, time can calculate, then experimental adjusting (dose. μjoule/cm^2)
5. Developing
   - There is a difference only in solubility, not soluble and insoluble areas
   - The developer is spayed on the surface usually
6. Burning (positive only)
7. Etching or electroplating

Manufacturing steps 3 - solid resists

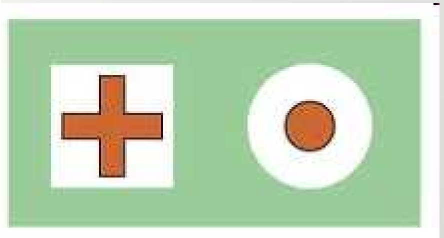
- **Du Pont – Riston film**
- **Laminating 100°C, (panel is preheated), surface is roughed**
- Exposition: **booth side together, precise positioning**
- Develop:
  - **Remove mylar film,**
  - **Developer is a weak alkaline solution (1 – 2%-os Na_2CO_3),**
  - **Spraying, need a mechanical impact**

Exposition methods

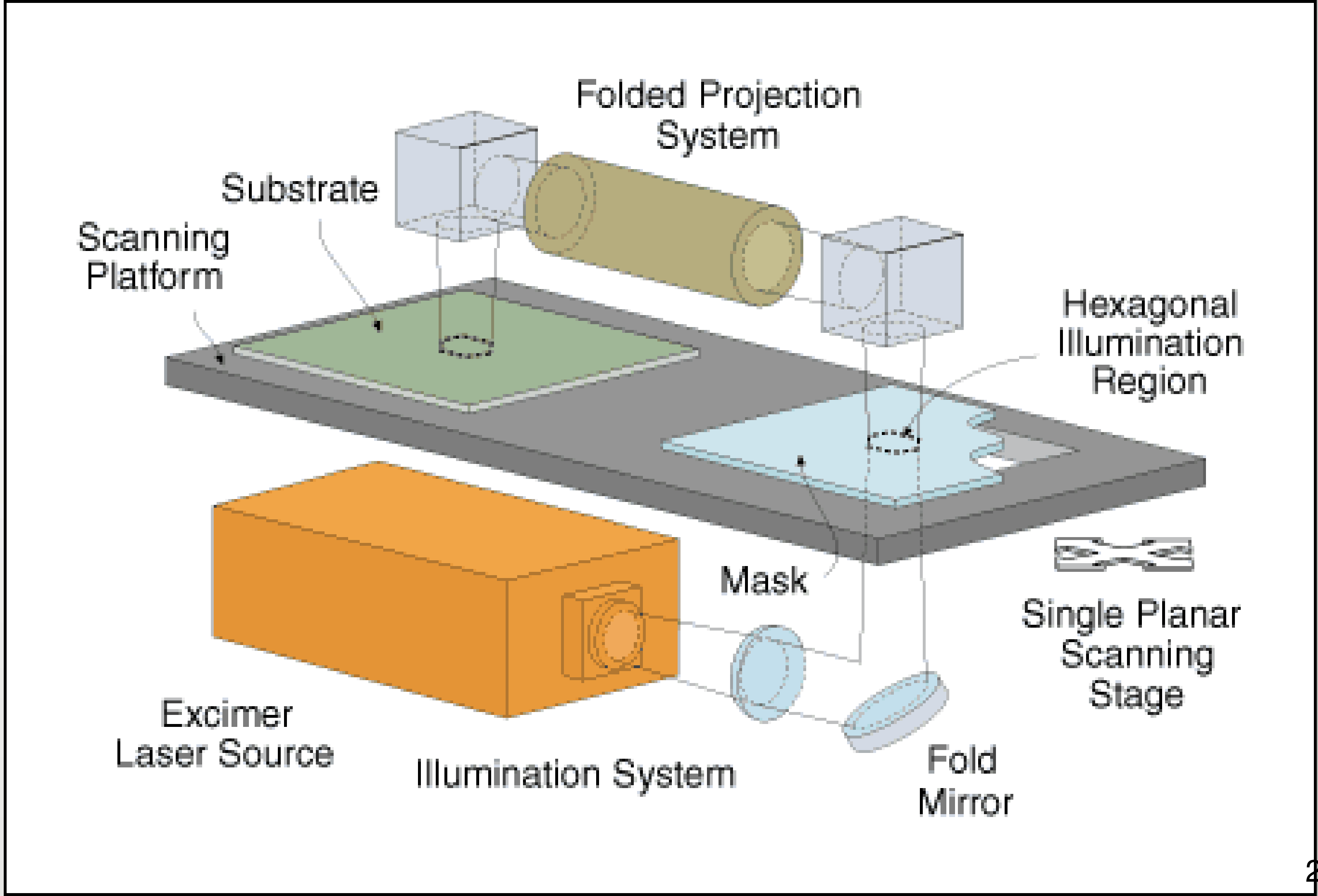
- Contact Imaging
- Laser Projection Imaging, LPI
- Laser Direct Imaging, LDI
- Step and Repeat Imaging

Contact Imaging

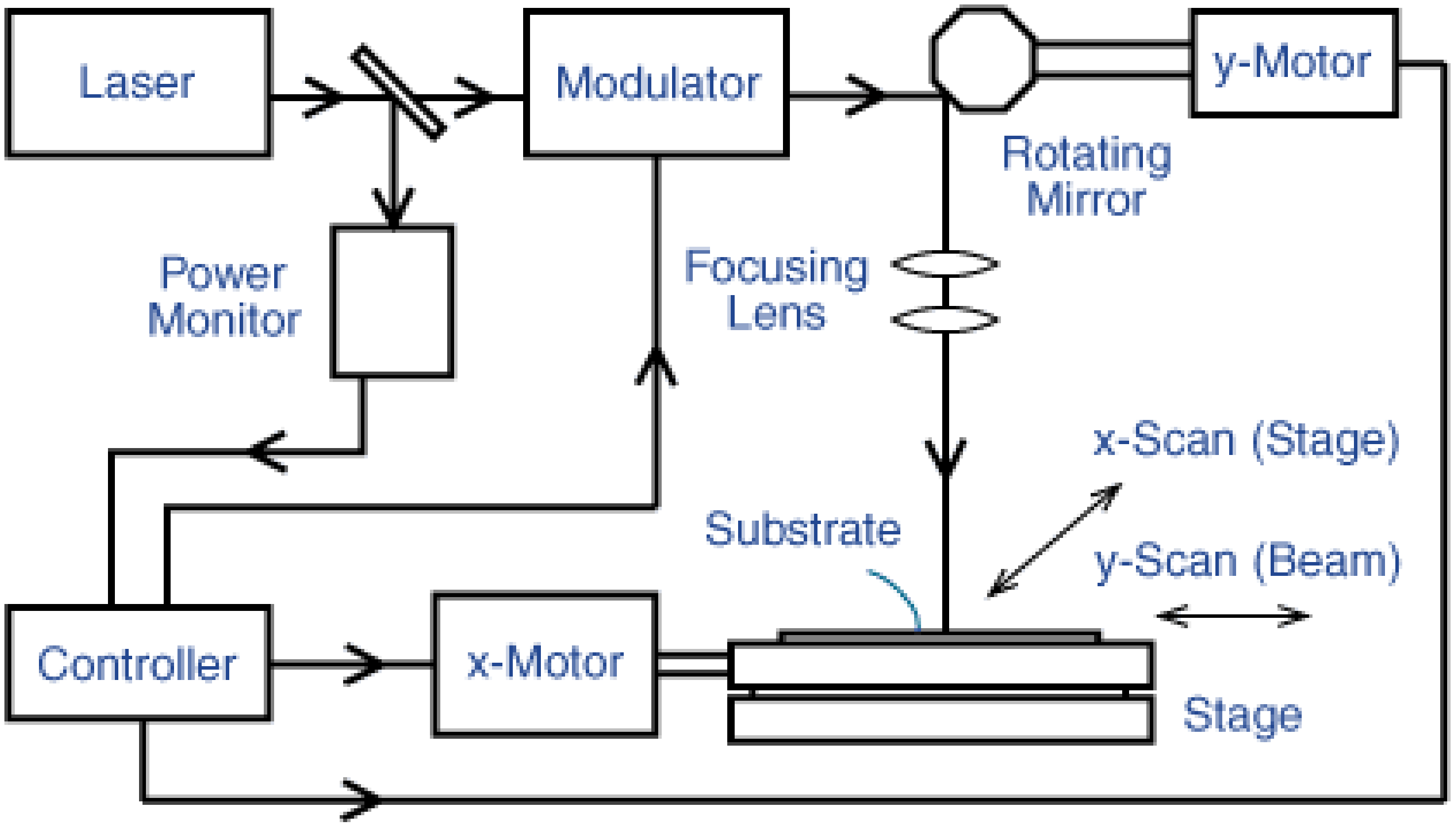
- Current, trouble-free processes,
- Cheap instruments,
- Good productivity,
- Low yield,
- Manual positioning is inaccurate,
- Low resoution (~100 µm),
- Mask wearing,
- Granular waste, dust causes troubles



Laser projection system



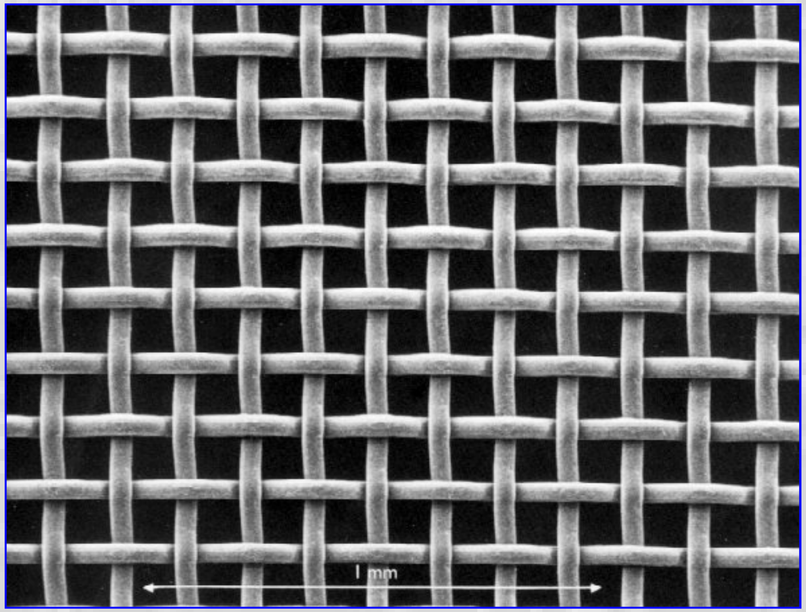
Laser direct imaging



Masking methods 2.

Screen printing

Applications:

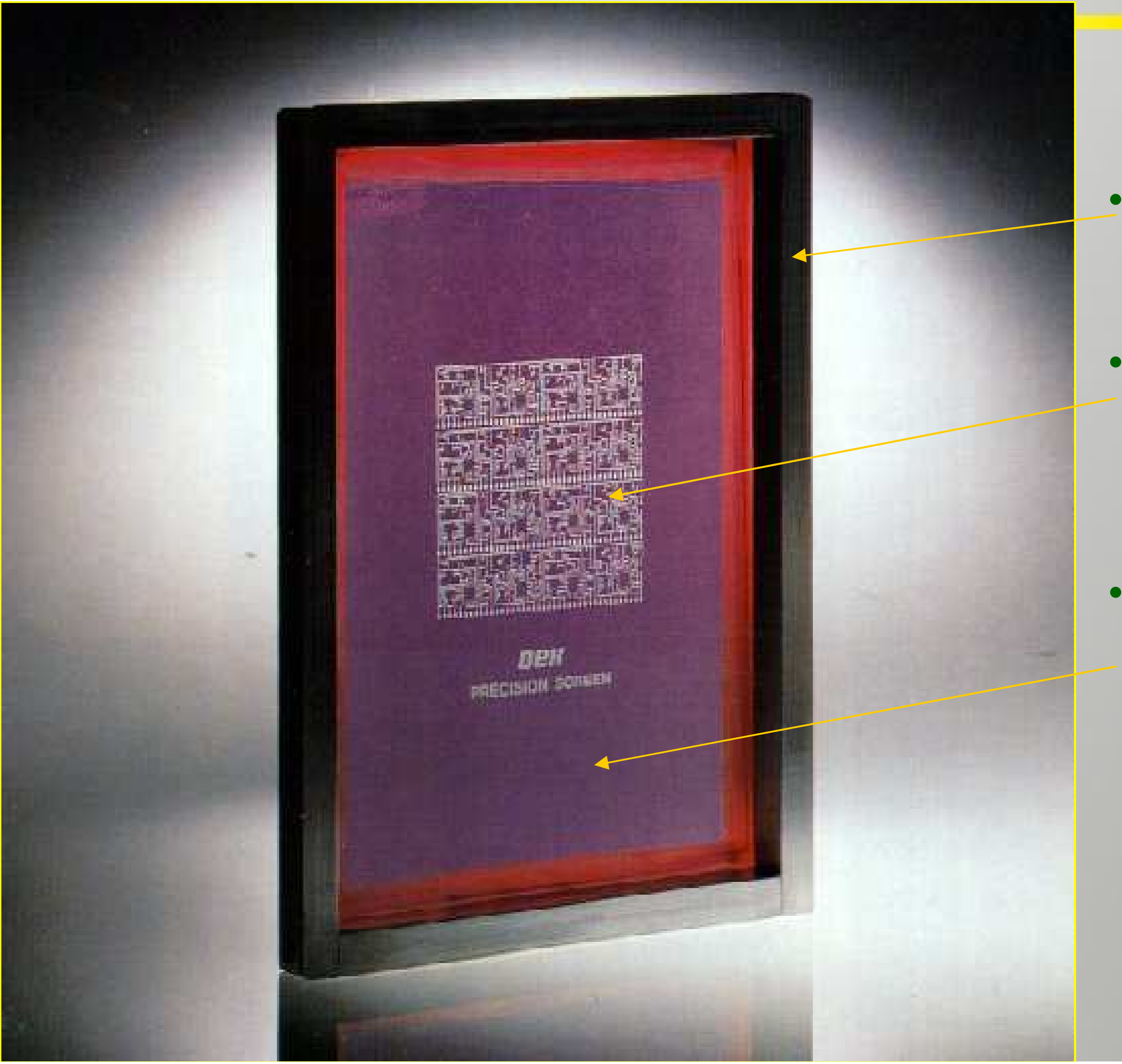


Medim or large volume production

Medium feature size

- Eatch-resist mask
- Solder paste
- Legend
- Uniform layers for photoimigeable liquids (solder mask)

Parts of the screen



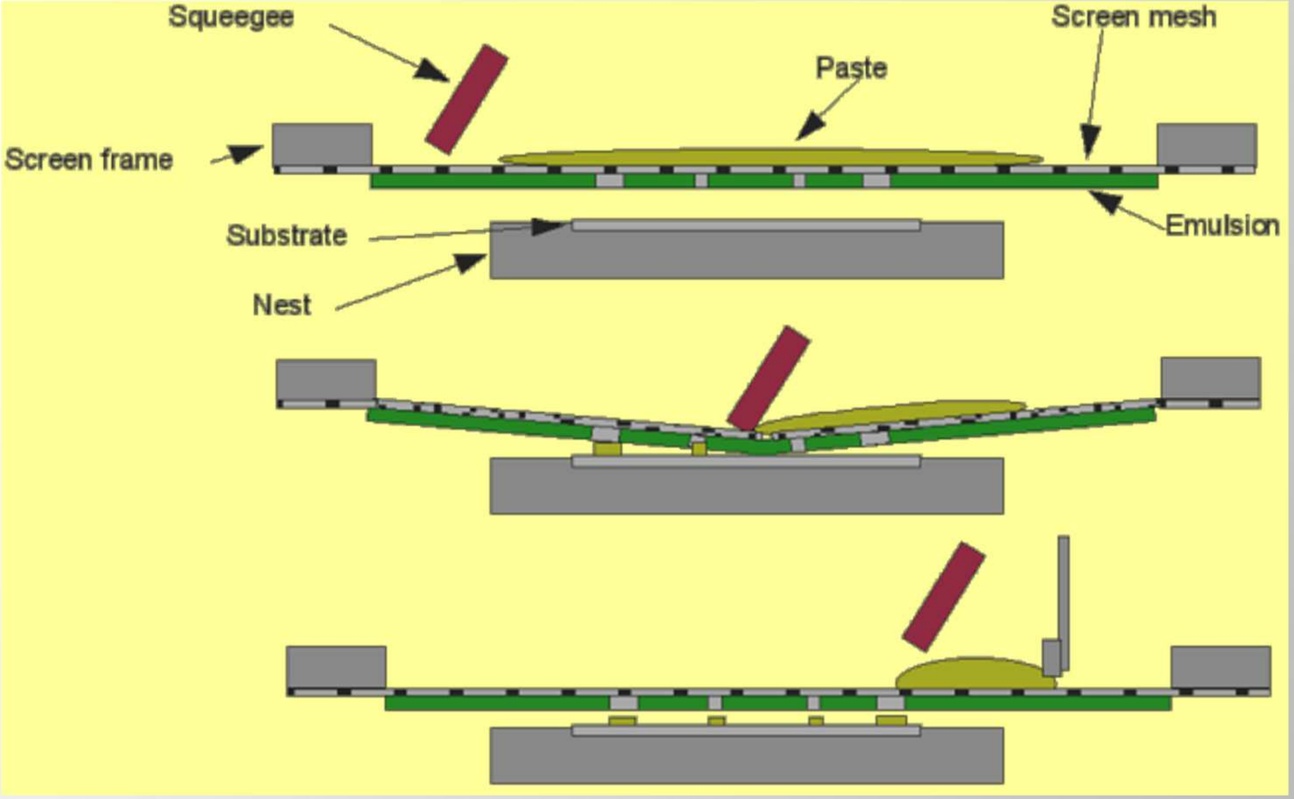
- Frame
- Emulsion mask
- Filler

Metal stencil

- Steel film, apertures cut by:
  - Laser
  - (Electrochemical) etching
  - Plasma etching
  - Galvanoplastic
- Benefits:
  - More precise,
  - Better resolution (127 – 65 μm fine pitch IC-s)
  - Longer lifespan (50 – 100 000 prints)
  - Good hardness and wear resistant

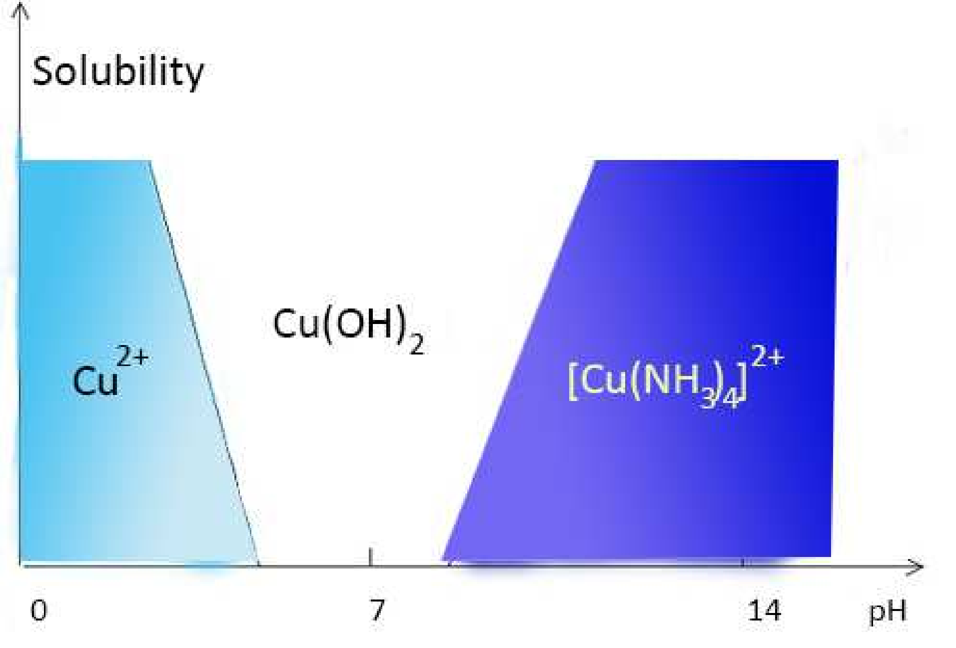
Suitable for solder paste printing

Printing



- Table: fixing, positioning, quick change of panels
- Squeegee:
    - sharp, chemically proof, wear-proof
    - Squeegee angle: 45 – 60°, *printing speed: medium slow*

Etching



- **Goal: removig copper from the uncovered areas.**
- **Etchant:**
  - Oxidativ: $Cu \rightarrow Cu^{2+} + 2e^-$
  - acid/alkaline pH: keep Cu^{2+} solved

Etchant types:

- *Acid:*

  sulfuric: Sulfuric acid – hydrogen-peroxide H_2SO_4

  ammonium-persulphate $(NH_4)_2S_2O_8$

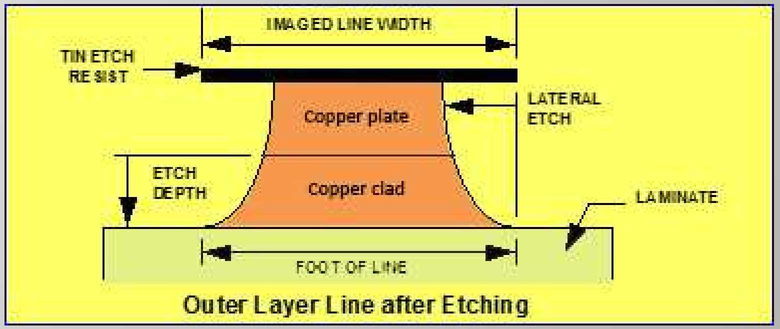
  chlorides: ferric chloride $FeCl_3$

  Copper(II)-chloride $CuCl_2$

- *Alkalic:* Copper-tetrammin complex $[Cu(NH_4)_4]^{2+}$

Etchant properties

- Rate of etching (μm/min)
  - Depends on the temperature and the solvent concentration
- Capacity (m²PCB/kg etchant)
- Undercut, etch factor: $(v_{\perp}/v_{||})$



- Selectivity (Sn mask on double layer PCB)
- Methode of regeneration
- Environmental and health impact

Etching methods

- Dipping
- Spray
- Jet stream
  - Always fresh etchant on the surface
  - Dissolved copper washed by heavy flow
  - Possibility of continuous regeneration (Copper recovery, redox potential and pH correction)
- Rinse
  - Minimal dropping out (air knife, rubber cylinder)
  - The first rinse water is dangerous waste
  - Cascade rinsing

PCB manufacturing 2

Metal layer preparation methods

Double side and multilayer PCB-s

High Density Interconnections

Making metal layers

Reduction: $Me^+ + e^- \rightarrow Me$

Electroless plating (Chemical reduction):

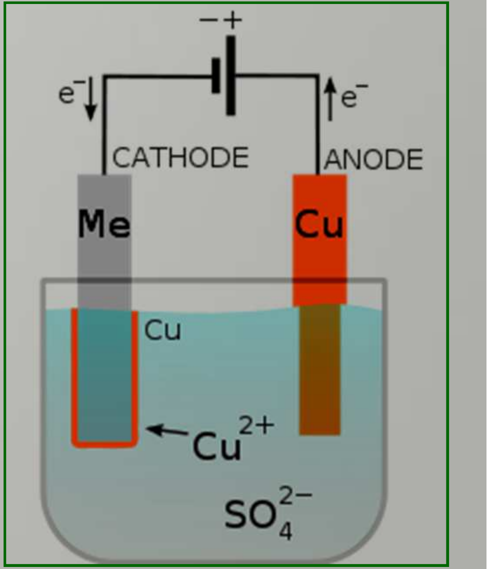
Suitable on insulating surfaces

- Application:
  hole metallization,
  resistors,
  Surface finishing
- Used materials: Cu, Ni, Ag

Galvanic plating

To the conductive surface only

- Application:
  Panel, drawing, connectors



Immersion plating:

Conductive surface, ion exchange reaction (The less active metal come out to the surface, more active go to the solution)

Used materials: Ag, Au

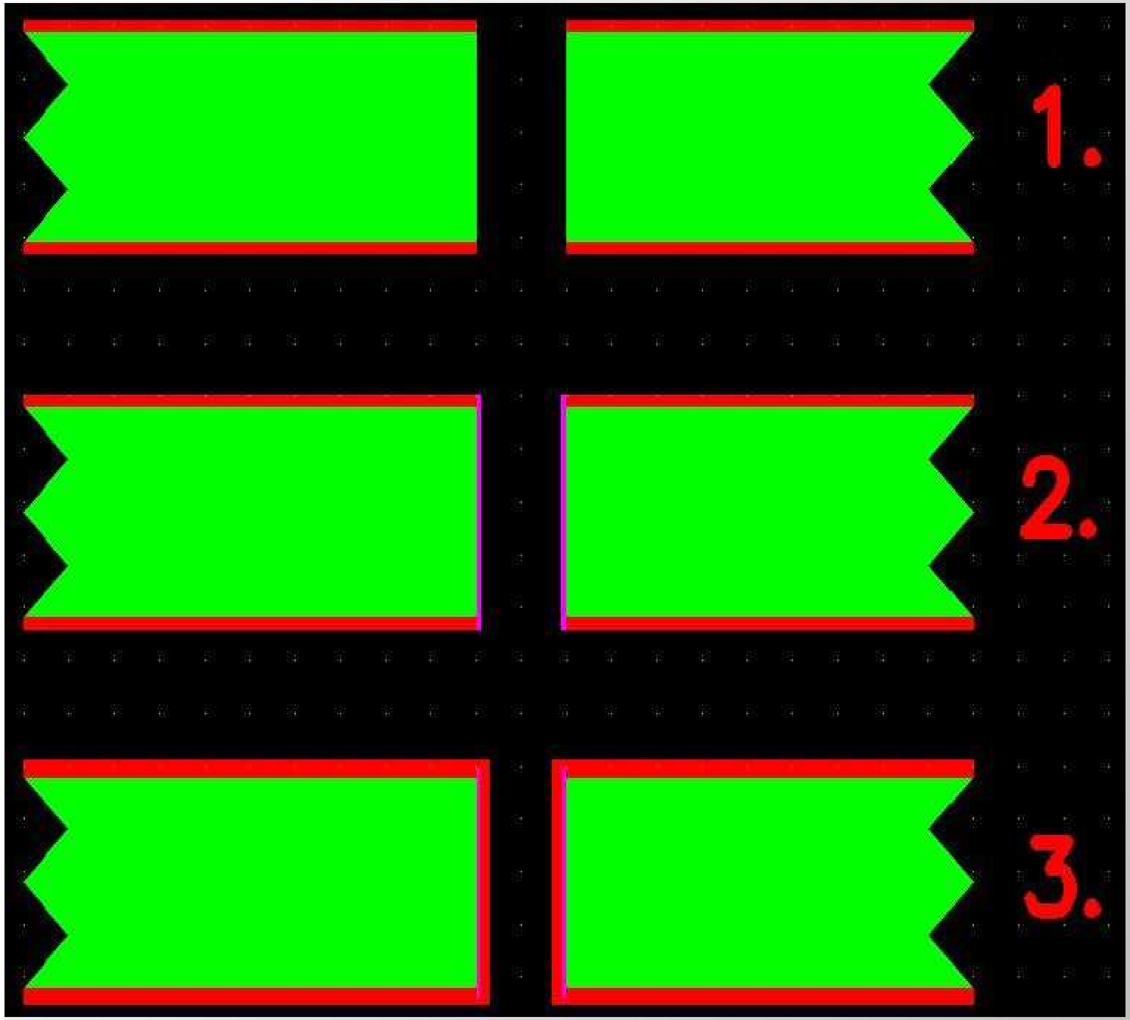
Electroless plating Processes:

- Surface peparation:
  - Clearing, degreasing
  - Microetching
  - Activation: first $SnCl_2$ then Pd
- Chemical reaction:

$$CuSO_4 + 2HCHO + 4NaOH \rightarrow Cu + 2(HCO)_2Na + H_2 + 2H_2O + Na_2SO_4$$

- At room temperature
- Layer thickness: 1-2μm, the surface turns conductiv, the plating continued by galvanic vay

Making hole conductive



- Electroless copper: (previous)
- Direct plating: base: thin Pd, then galvanic copper
- Black hole: grafit suspension → galvanic Cu
- Conductive polymer: polymer layer – oxidation, turn conductive → galvanic Cu

Copper galvanic plating applications

- Hole metallization (panel, drawing)
- Intermediate layer (improve adhesion, diffusion barrier)
- Acid bath: $CuSO_4 + H_2SO_4 + NaCl +$ additives
- $j = 0{,}5 \ldots 5 A/dm^2$, agitations of cathode,
- anode: phosphorus dopant copper

Other metallisation processes

Immersion plating

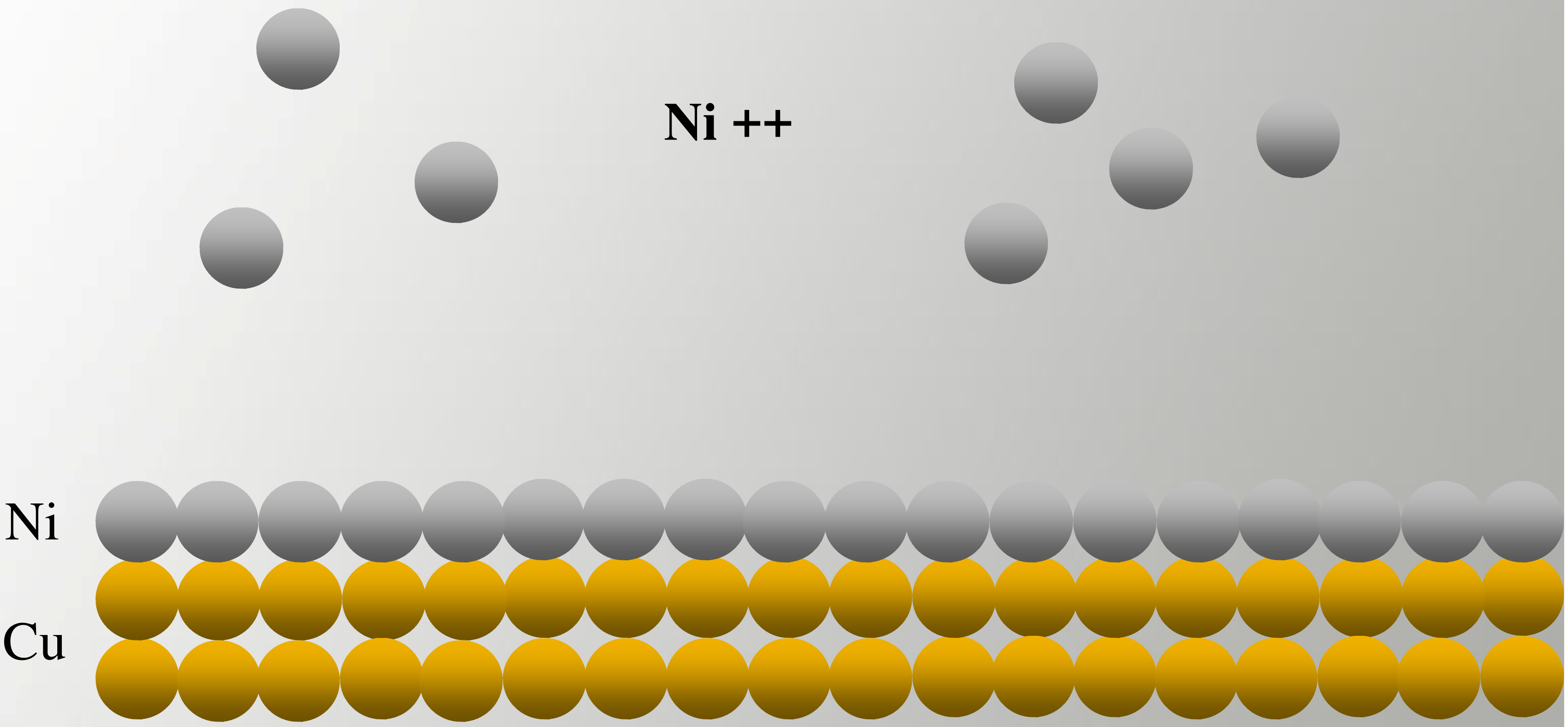
- Gold, silver
- Improve wettability of the surface for soldering
- Ion exchange:
    - eg: ENIG (electroless nickel, immersion gold)

$$Ni + Au^{2+} \rightarrow Ni^{2+} + Au$$

~0,1 µm, self stop reaction

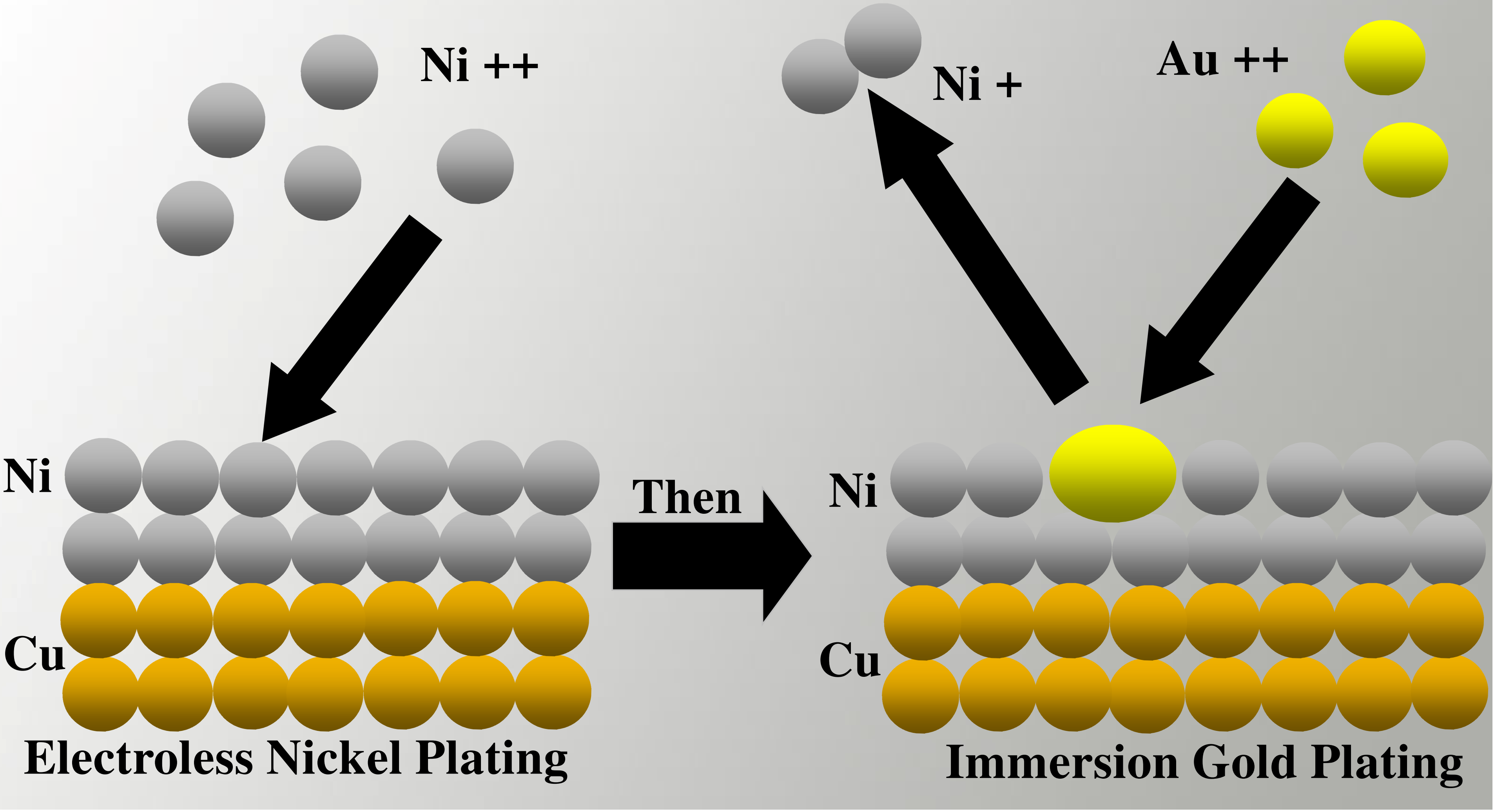
Electroless Plating

Electroless Nickel



Electroless and Immersion Plating

ENIG



02.27.

HASL

Hot Air
Solder
Levelling

Cross section of a via

Plated hole

Formation a mushroom

Sumary of the double side PCB technology

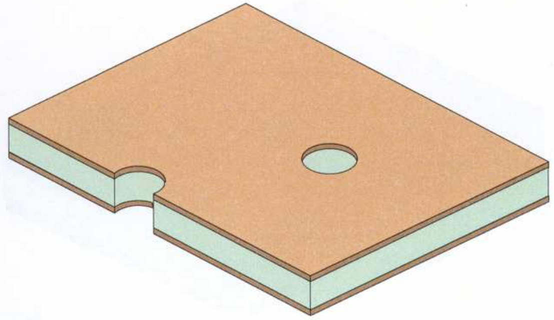


Illustration DS-2. **Drill.** Hole sizes and location are determined by drill data furnished by customer.

36 MANUFACTURING PCBs

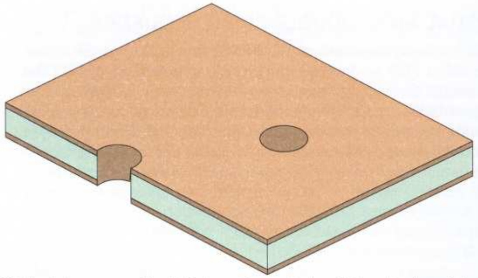


Illustration DS-3. **Electroless copper plate.** A thin layer of copper is deposited on all surfaces including the walls of the drilled holes.

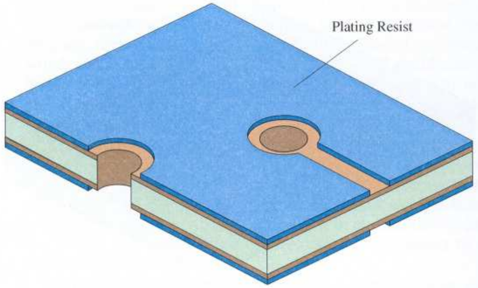


Illustration DS-4. **Apply plating resist.** The desired circuitry is left uncovered.

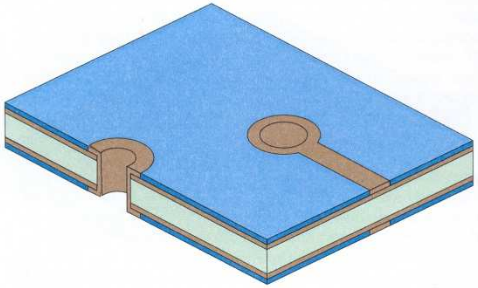


Illustration DS-5. **Electroplate copper.** The specified thickness is electrolytically deposited (usually 0.0015″).

- Drilling
- Activation Sn → Pd - electroless Cu – galvanic Cu – panel-plating ~5 μm
- Solid photoresist lamiation – Photolithography – negative mask
- Galvanic Cu → 20μm

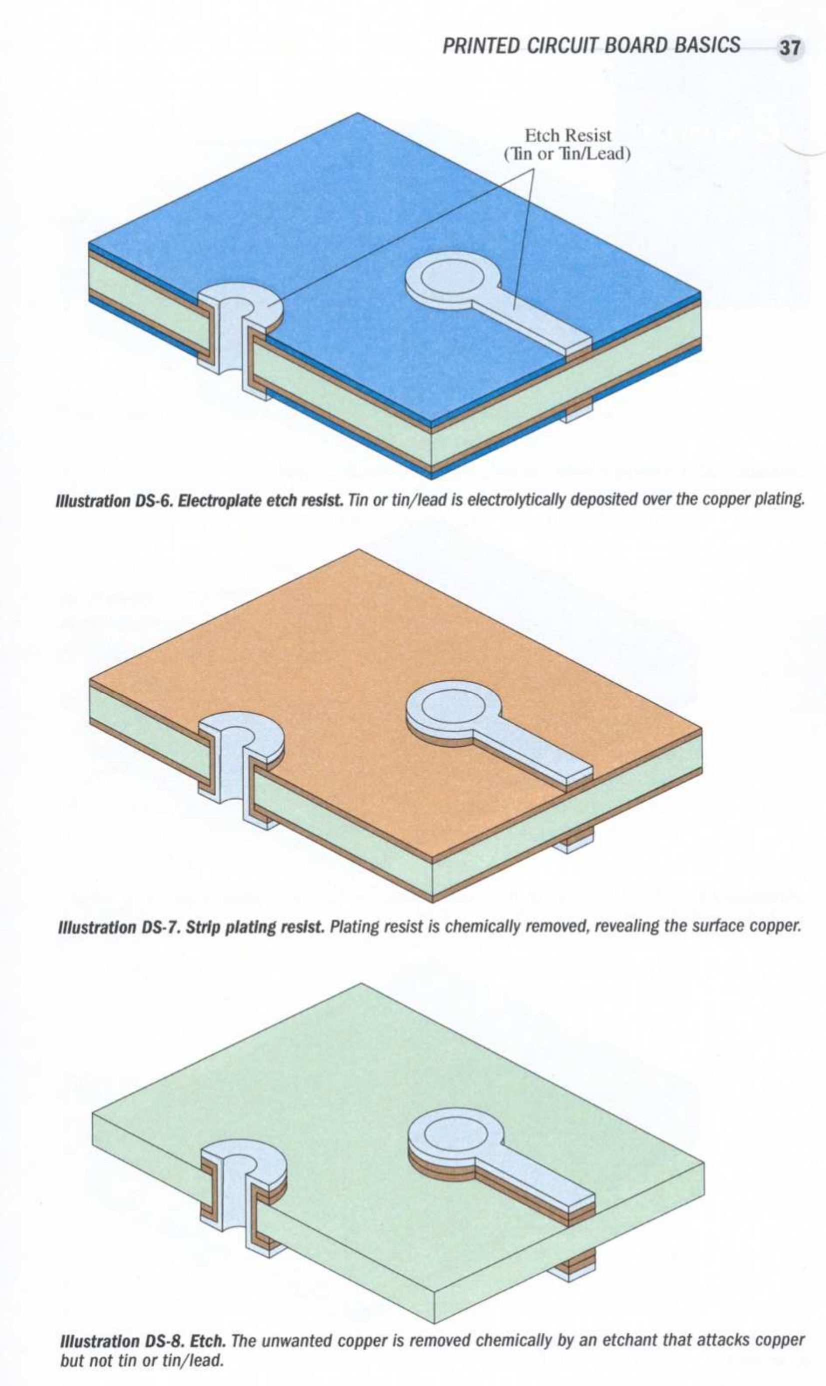
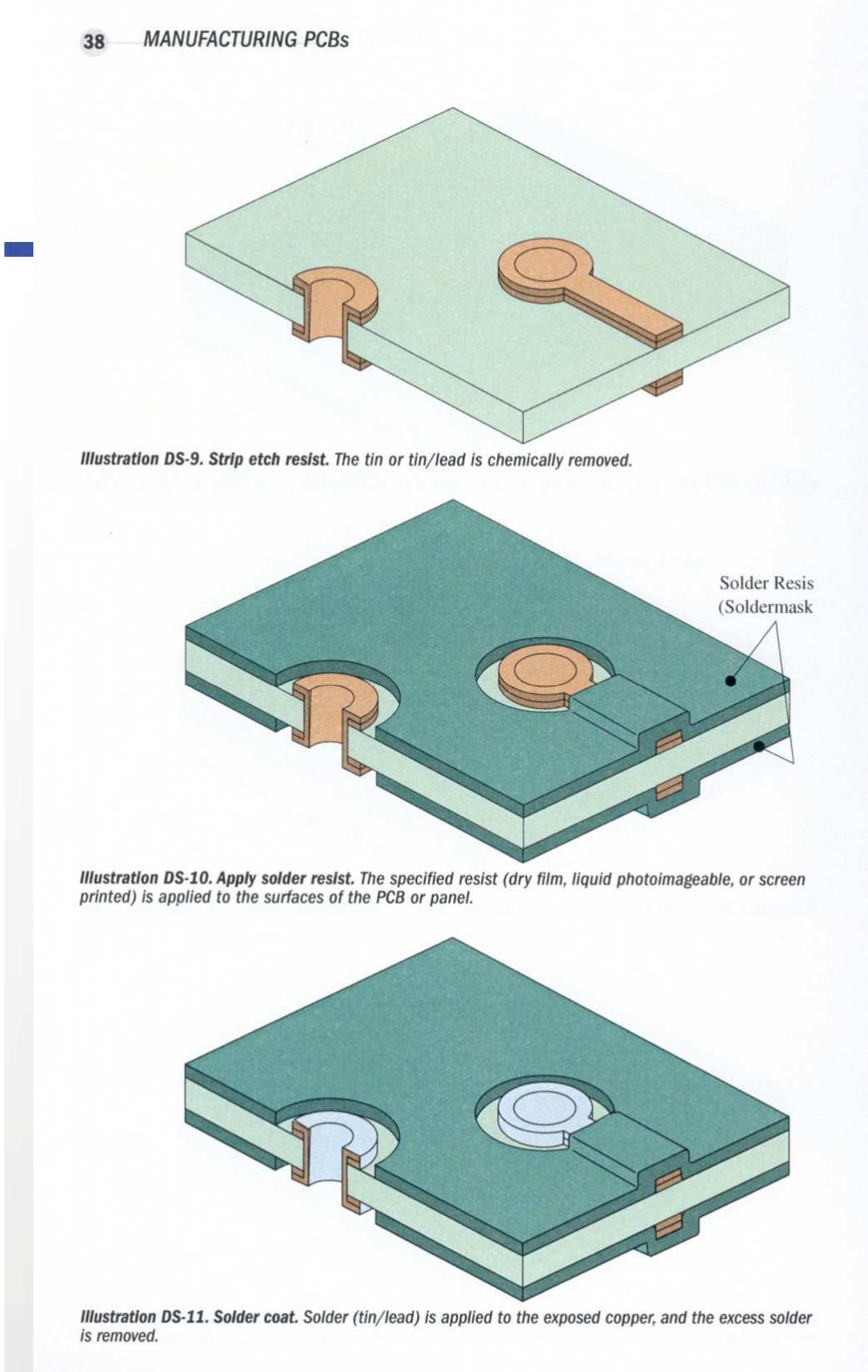

PRINTED CIRCUIT BOARD BASICS 37

Illustration DS-6. Electroplate etch resist. *Tin or tin/lead is electrolytically deposited over the copper plating.*

Illustration DS-7. Strip plating resist. *Plating resist is chemically removed, revealing the surface copper.*

Illustration DS-8. Etch. *The unwanted copper is removed chemically by an etchant that attacks copper but not tin or tin/lead.*

- **Galvanic Sn (~10μm)**
- **Stripping**
- **Selectiv etching**



38 MANUFACTURING PCBs

Illustration DS-9. Strip etch resist. *The tin or tin/lead is chemically removed.*

Illustration DS-10. Apply solder resist. *The specified resist (dry film, liquid photoimageable, or screen printed) is applied to the surfaces of the PCB or panel.*

Illustration DS-11. Solder coat. *Solder (tin/lead) is applied to the exposed copper, and the excess solder is removed.*

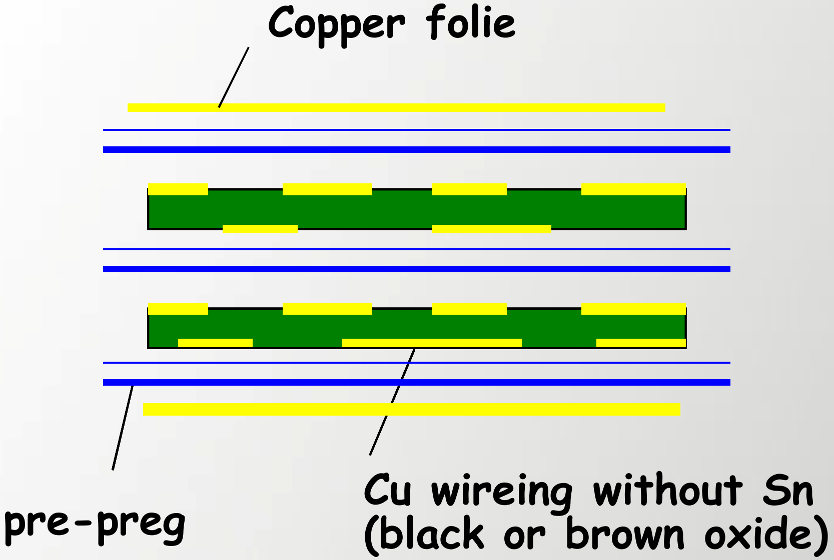
- **Removing Sn layer**

- **Soldermask**

- **Surface finishing (Au, Ag, Sn, OSP)**

Multilayer PCB

Six-layer packet



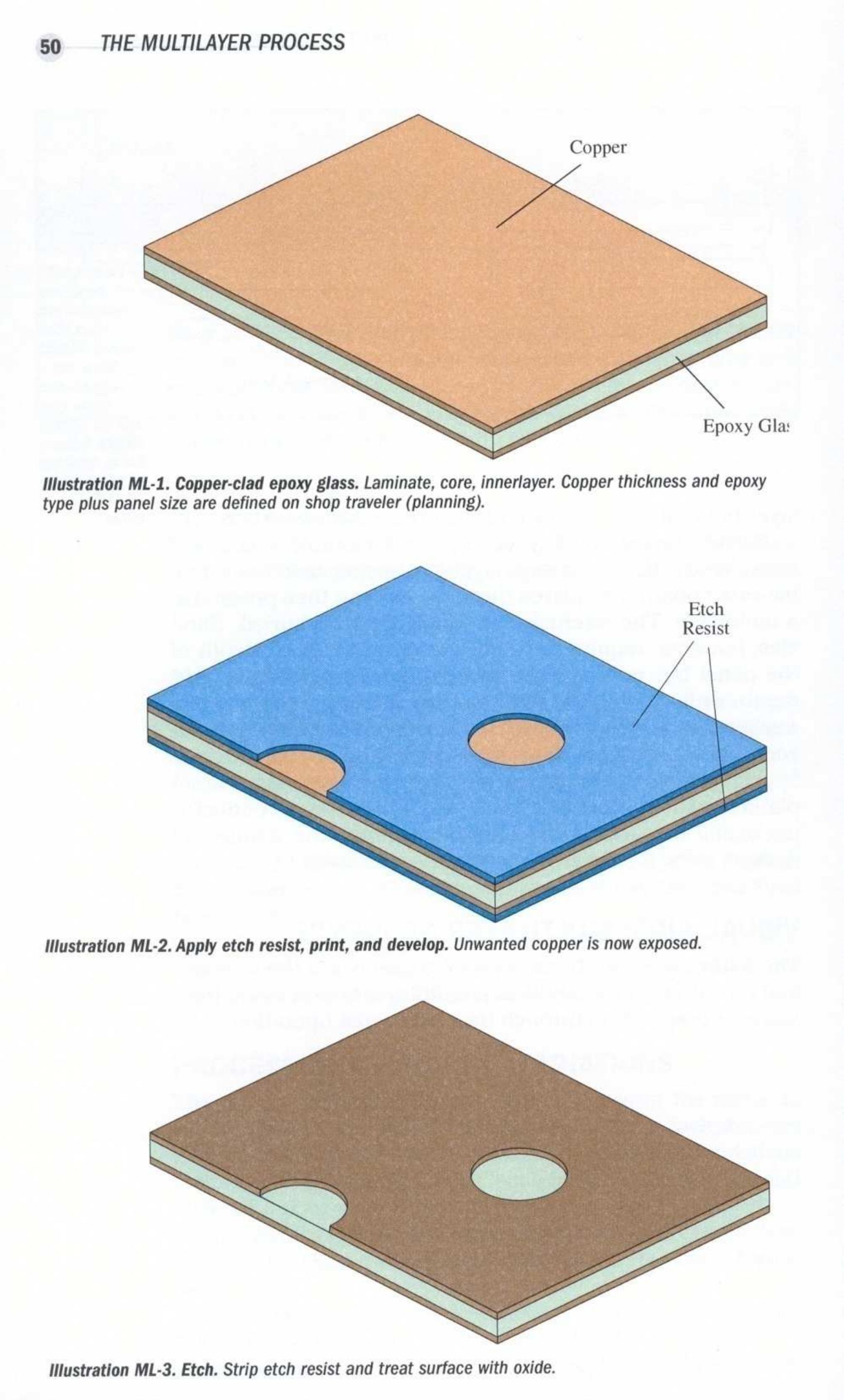
Pre-preg: preimpregnated material, half-hardened, glass-textile reinforced epoxi (the same material as the substrate)

Co-laminated methode

- Inner layers: Double side boards, Cu thickness 35 μm. The artwork prepared one by one, without holes
- Thin copper-oxide layer, to improve adhesion
- Top and bottom layer: plain Cu folie
- Packet: precise positioning with the help of studs (sticks).
- Hot pressing: 170°C, 15bar, 40-60 min
- Drilling, hole plating, photolitography … like at the double side PCB
- Mainly through holes

- **Summary of coo-laminated multilayer technology**

- http://www.pcb007.com/pages/pcb007.cgi
- http://www.hdihandbook.com/
- http://flexiblecircuittechnology.com/flex4/



50 THE MULTILAYER PROCESS

Illustration ML-1. Copper-clad epoxy glass. *Laminate, core, innerlayer. Copper thickness and epoxy type plus panel size are defined on shop traveler (planning).*

Illustration ML-2. Apply etch resist, print, and develop. Unwanted copper is now exposed.

Illustration ML-3. Etch. Strip etch resist and treat surface with oxide.

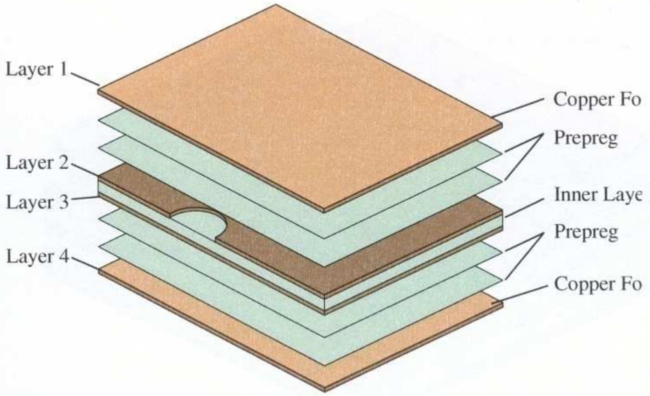


Illustration ML-4. Layup. *Four-layer multilayer using foil lamination technique. Foil, prepreg type, and size is defined on shop traveler.*

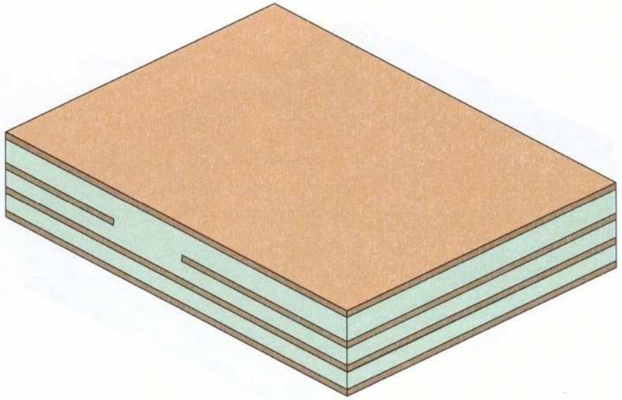


Illustration ML-5. Laminate. *Heat and pressure cause prepreg to flow and bond layers together.*

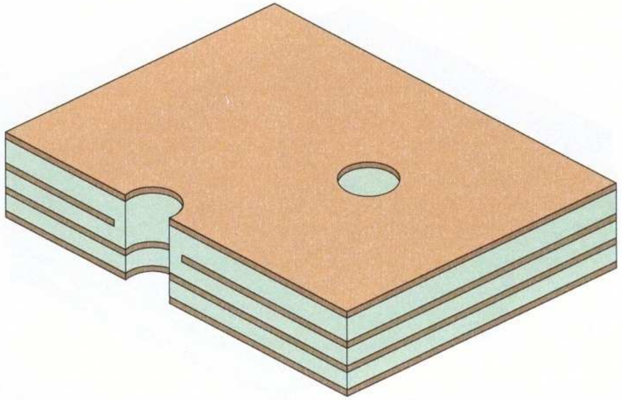


Illustration ML-6. Drill. *Hole sizes and location are determined by drill data furnished by customer.*

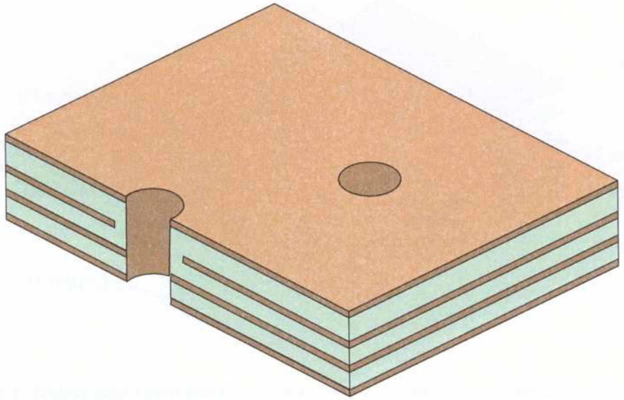


Illustration ML-7. Electroless copper plate. *A thin layer of copper is deposited following smear removal, cleaning, and preparation.*

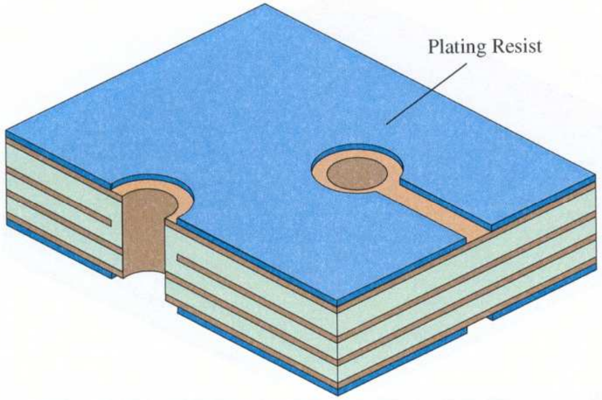


Illustration ML-8. Apply plating resist. *The desired circuitry is left uncovered.*

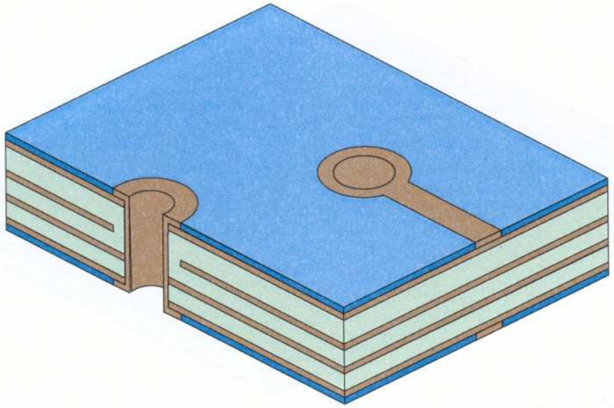


Illustration ML-9. Electroplate copper. *The specified thickness is electrolytically deposited (usually 0.0015″).*

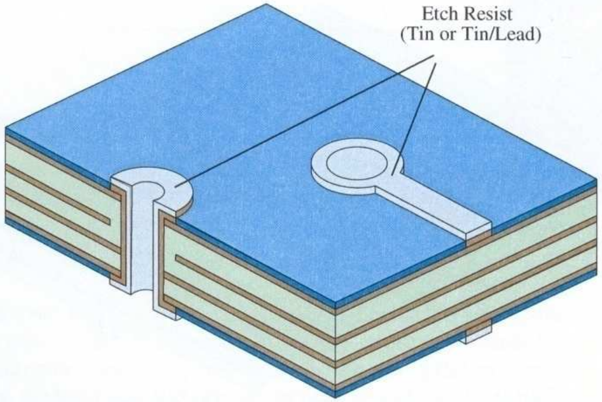


Illustration ML-10. Electroplate etch resist. *Tin or tin/lead is electrolytically deposited over the copper plating.*

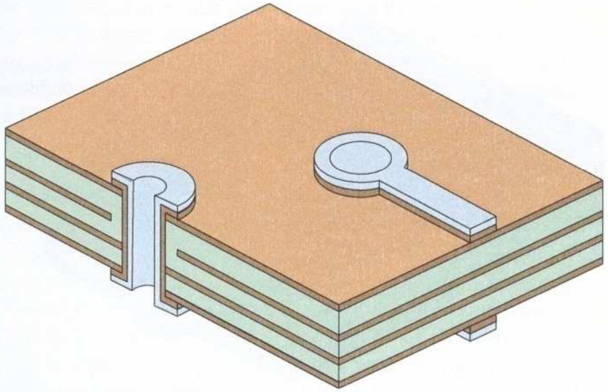


Illustration ML-11. Strip plating resist. *Plating resist is chemically removed, revealing the copper surface.*

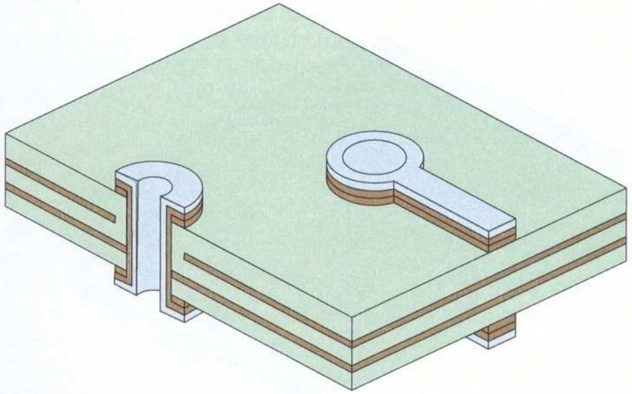


Illustration ML-12. Etch. *The unwanted copper is removed chemically by an etchant that attacks copper but not tin or tin/lead.*

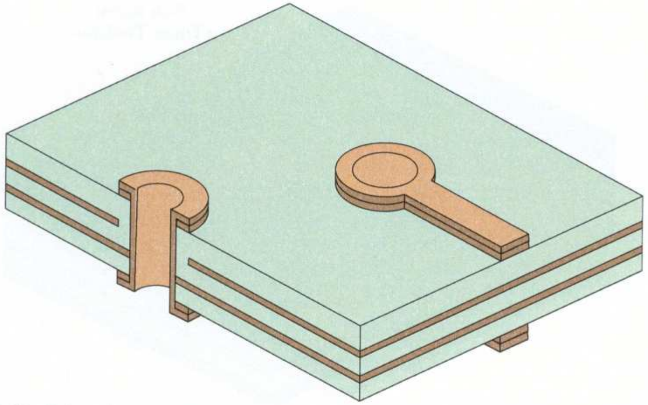


Illustration ML-13. Strip etch resist. *The tin or tin/lead is chemically removed.*

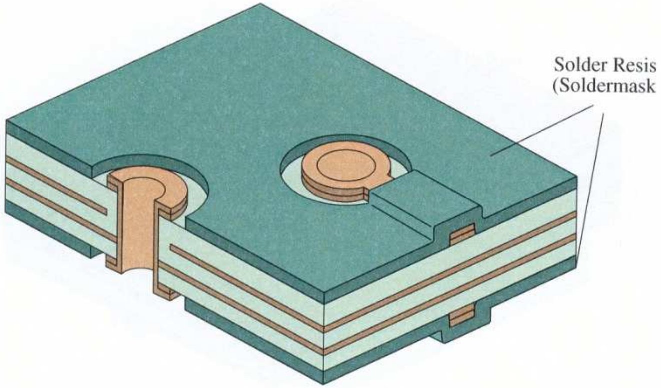


Illustration ML-14. Apply solder resist. *The specified resist (either dry film, liquid photoimageable, or screen printed) is applied to the surfaces of the PCB or panel.*

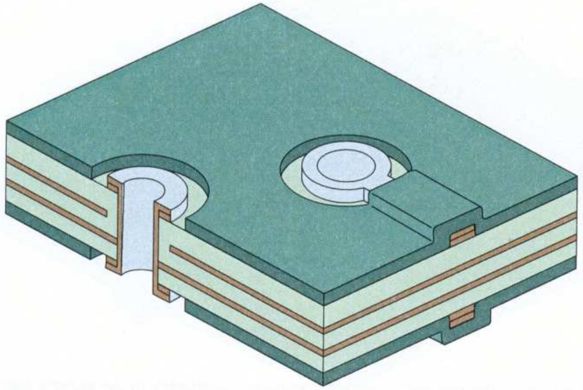
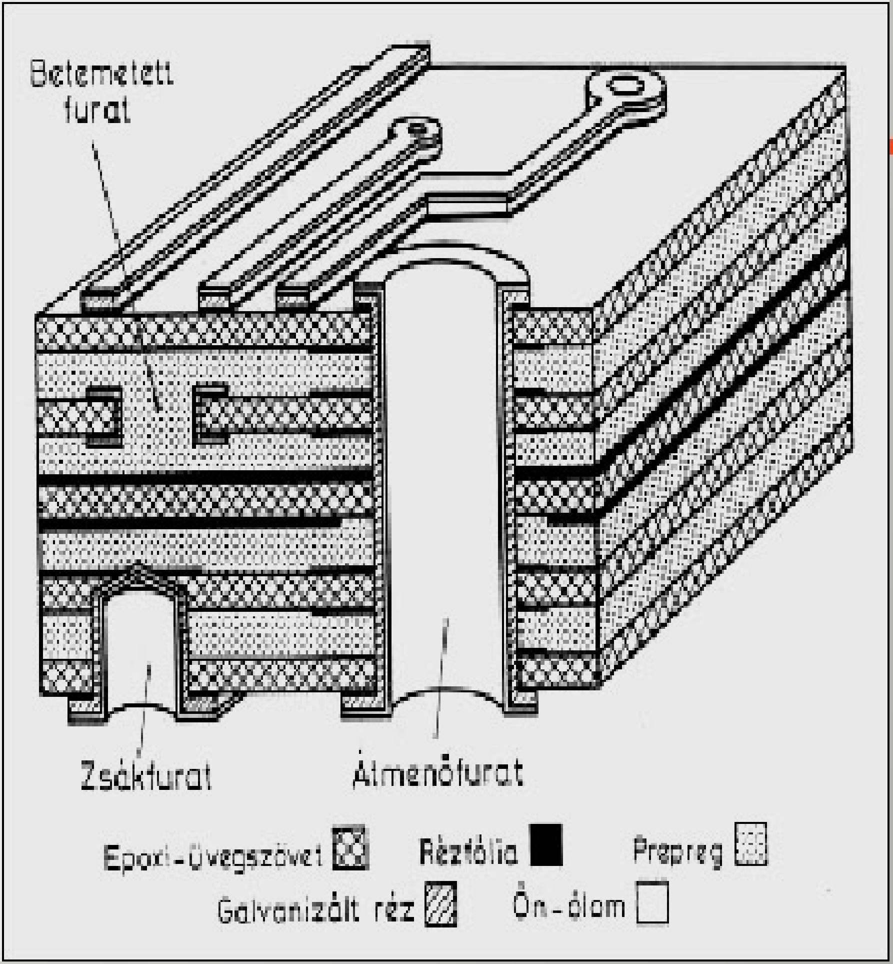
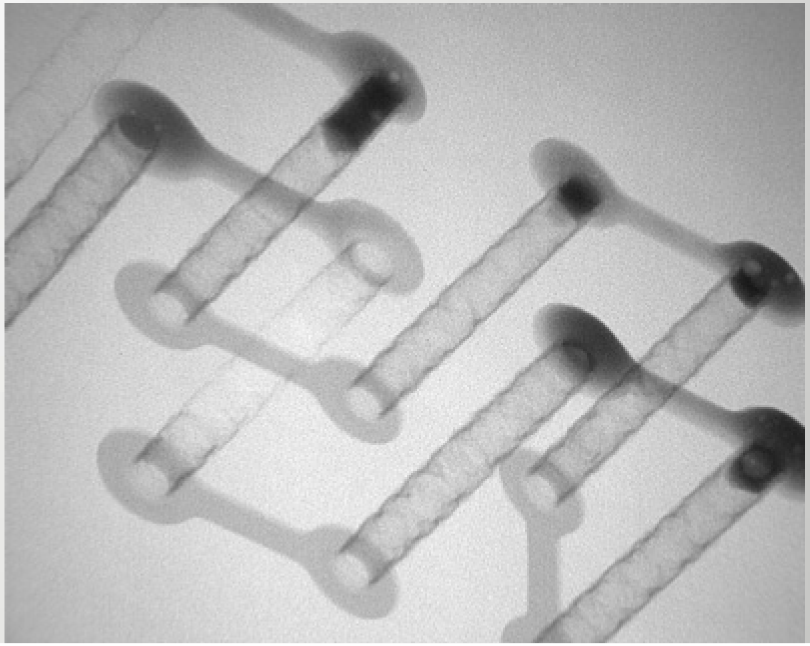


Illustration ML-15. Solder coat. *Solder (tin/lead) is applied to the exposed copper areas, and the excell solder is removed.*

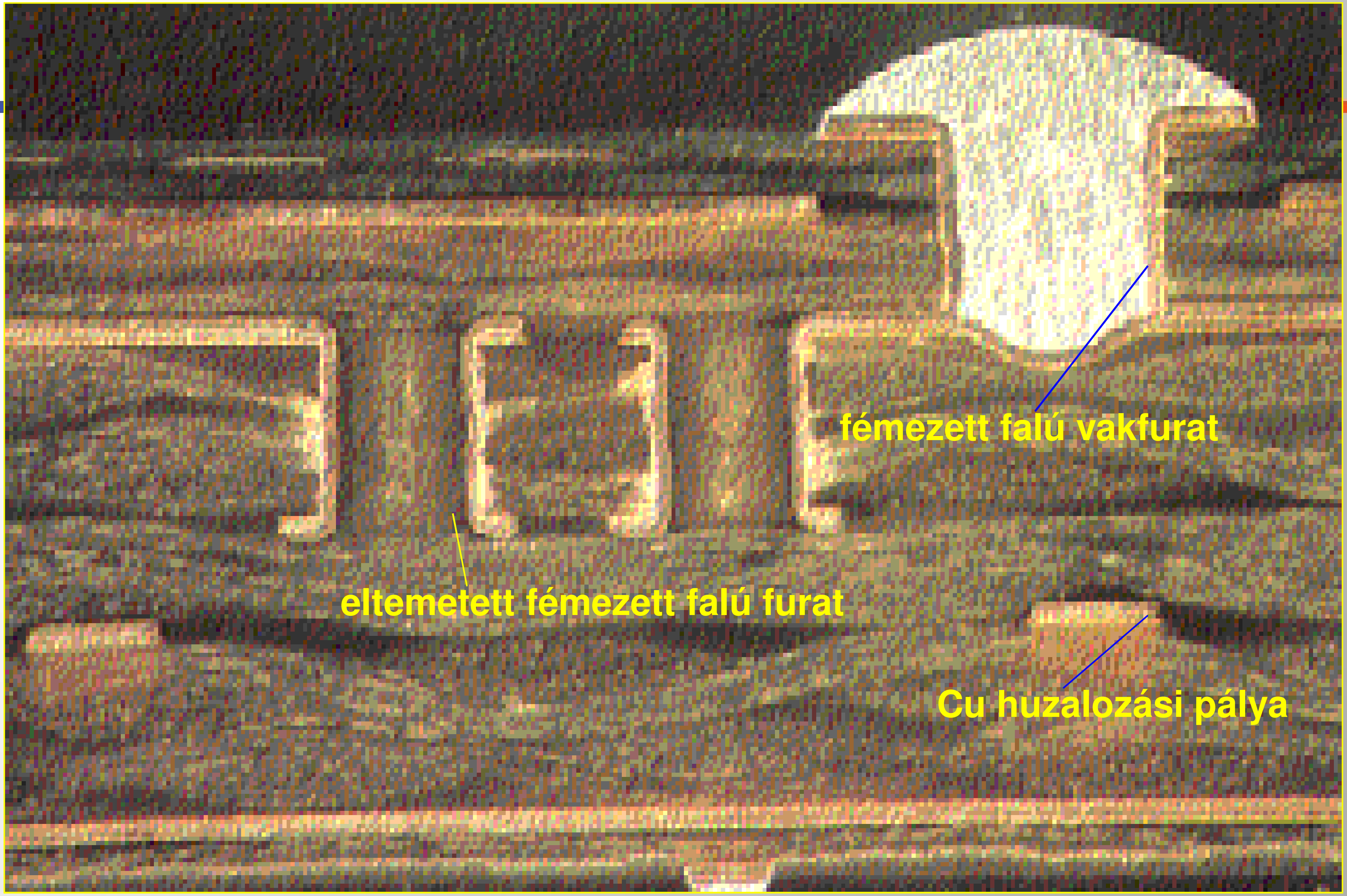
Blind and buried vias:

Difficult to make in this methode. Prepared in the single inner boards.



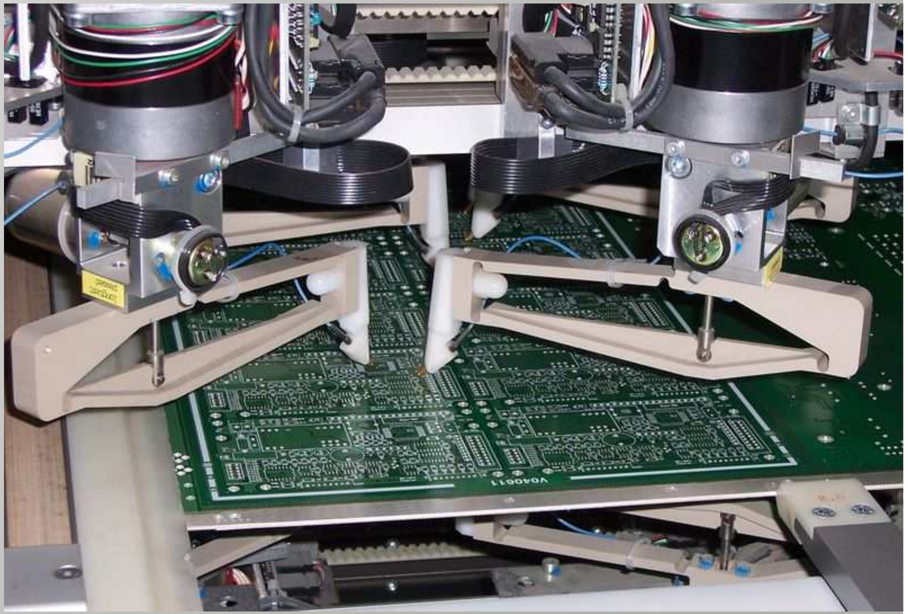


X-ray image of plated through holes


fémezett falú vakfurat
eltemetett fémezett falú furat
Cu huzalozási pálya

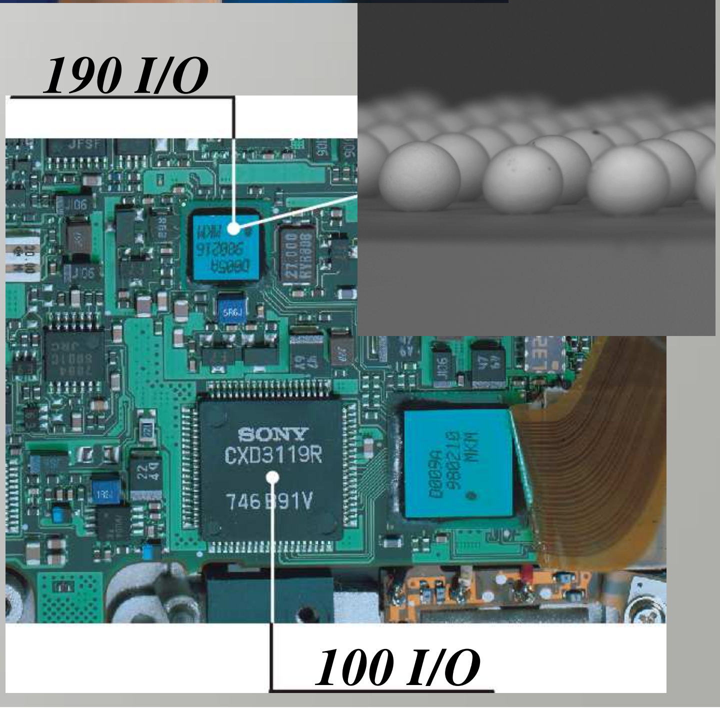
Quality control

- **Systemahic control during the production**
  - **Control of tools: Drill bits, chemicals, baths, electrodes**
  - **Control of intermediates and products**
  - **Main methodes:**
    - *Visual*
    - *AOI: Automatical Optical Inspection*
    - *Test automats*



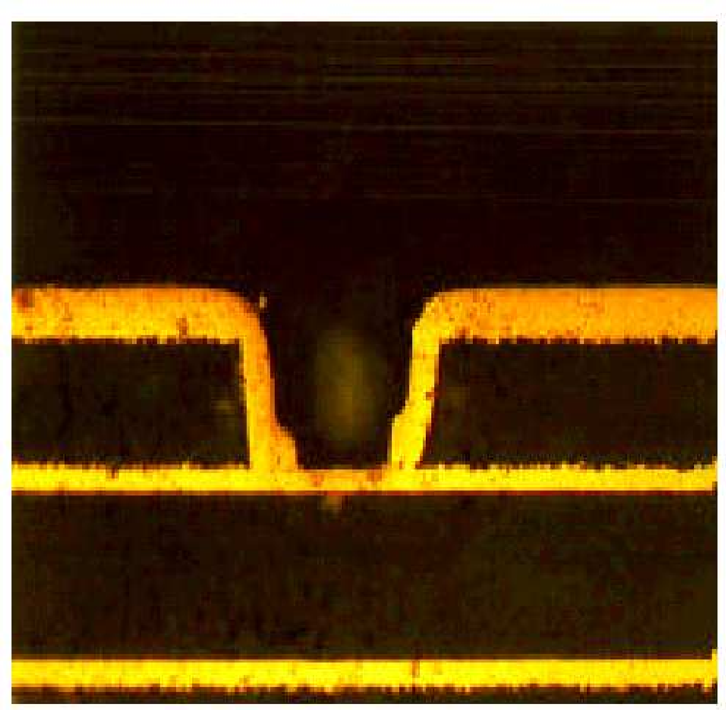
HDI: High Density Interconnection

- Line width < 150μm
- Microvias (buried, blind)
  d < 0,3 mm,
  more than 1000 holes/dm^2
- Sequential technologie
- Embedded passive components



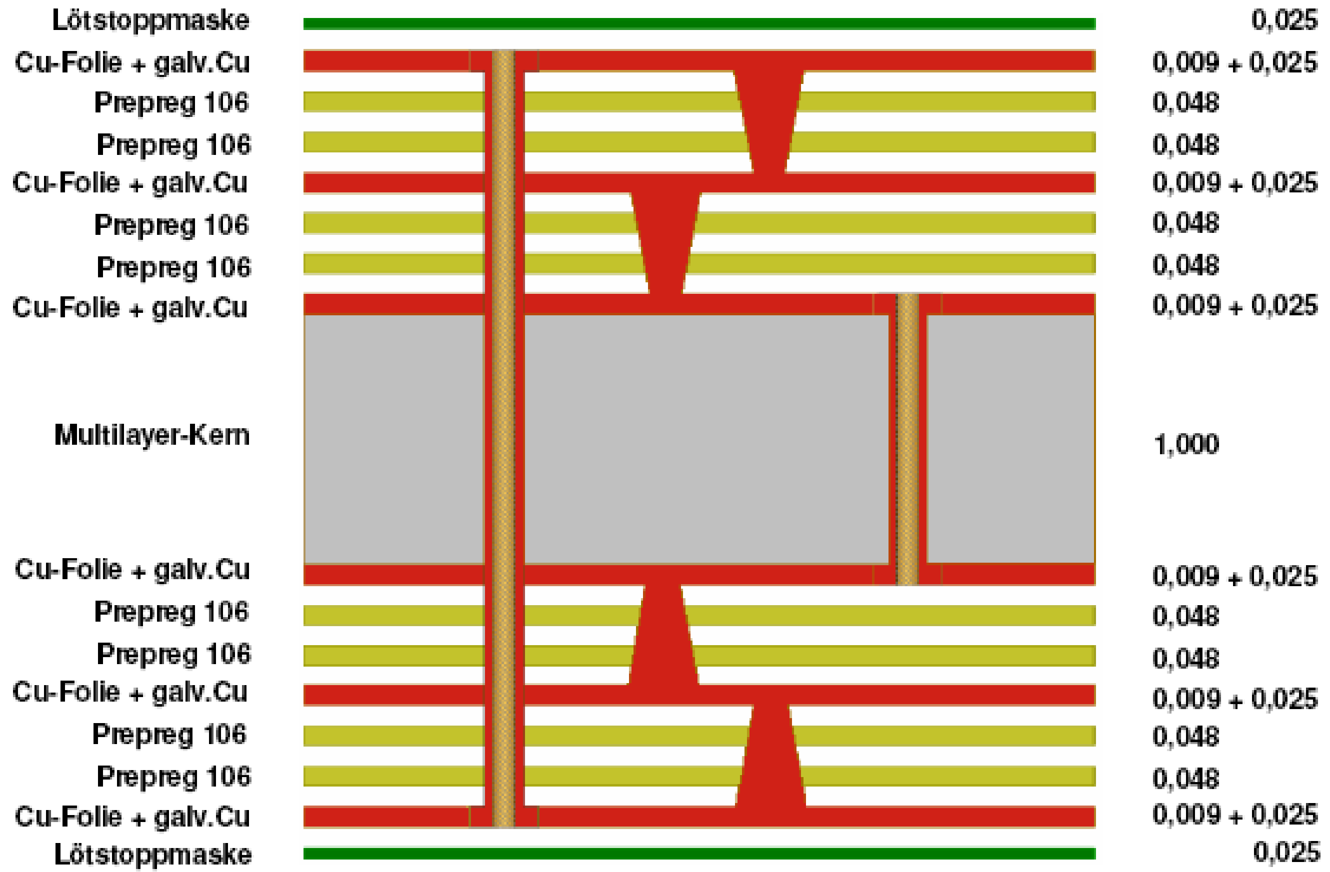
Sequential technology, microvia

- Sequential: build up layer by layer
- Microvia: 10…100μm diameter, drilling by laser or plasma etching
- Benefits: smaller board, higher speed, less layers, lower price



Plated blind via

Multilayer board, base board and 2 + 2 sequential layers



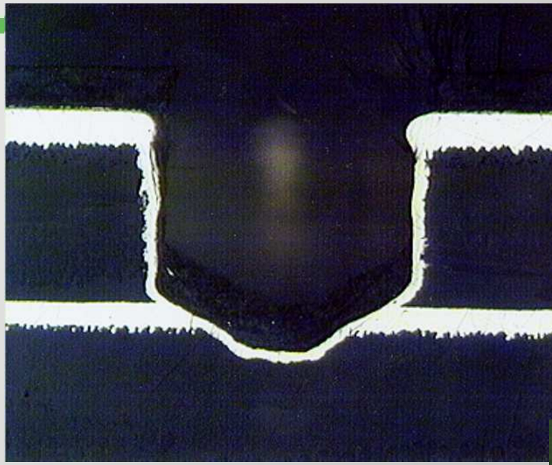
Lötstoppmaske	0,025
Cu-Folie + galv.Cu	0,009 + 0,025
Prepreg 106	0,048
Prepreg 106	0,048
Cu-Folie + galv.Cu	0,009 + 0,025
Prepreg 106	0,048
Prepreg 106	0,048
Cu-Folie + galv.Cu	0,009 + 0,025
Multilayer-Kern	1,000
Cu-Folie + galv.Cu	0,009 + 0,025
Prepreg 106	0,048
Prepreg 106	0,048
Cu-Folie + galv.Cu	0,009 + 0,025
Prepreg 106	0,048
Prepreg 106	0,048
Cu-Folie + galv.Cu	0,009 + 0,025
Lötstoppmaske	0,025

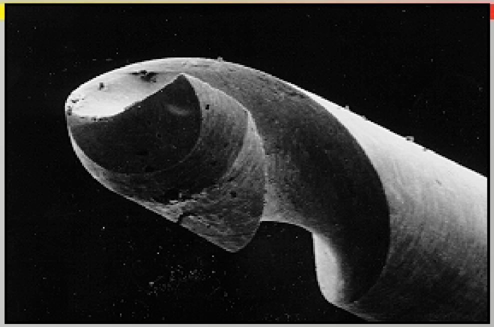
Presslingsdicke : 1,55 +/-10%

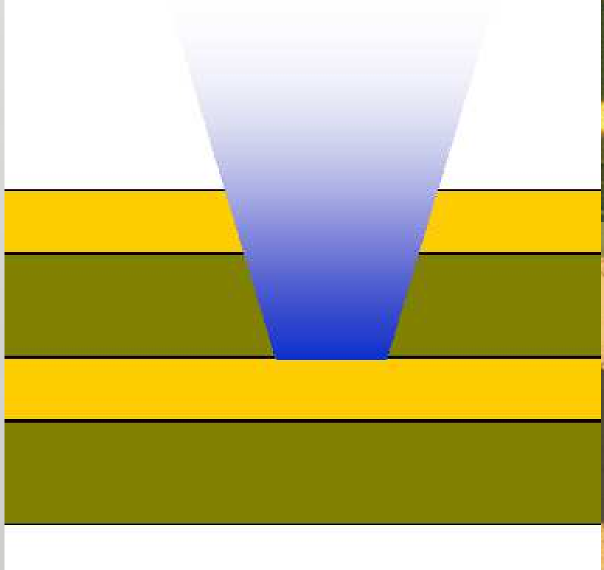
Gesamtdicke inklusive galvanischer Aufkupferung und Lötstoppmaske : 1,68 +/-10%

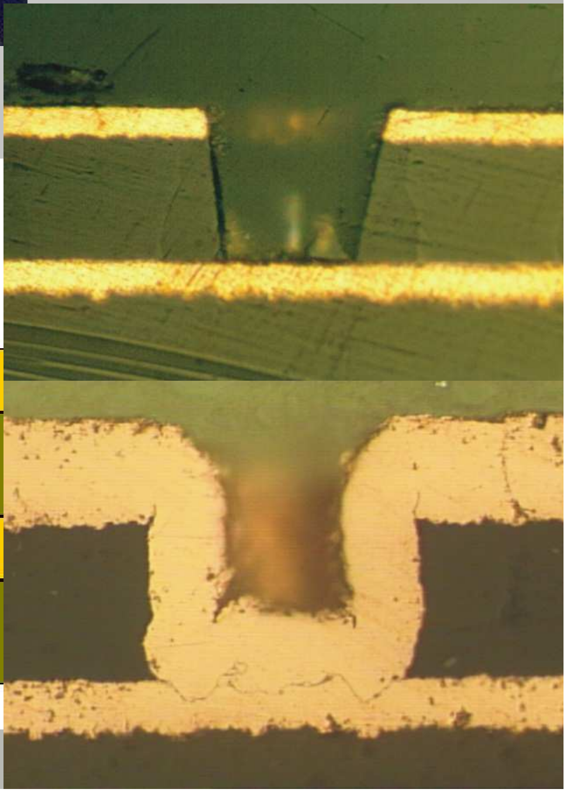
Microvia drilling

- **Mechanical:**
  reduced accuracy:
  z axis: ~ 40 µm,
  side: ~ 50 µm
- **Plasma**
- **Laser**
  - CO_2 laser 10,6µm (not for metals)
  - UV laser
  - d ~ 30 µm

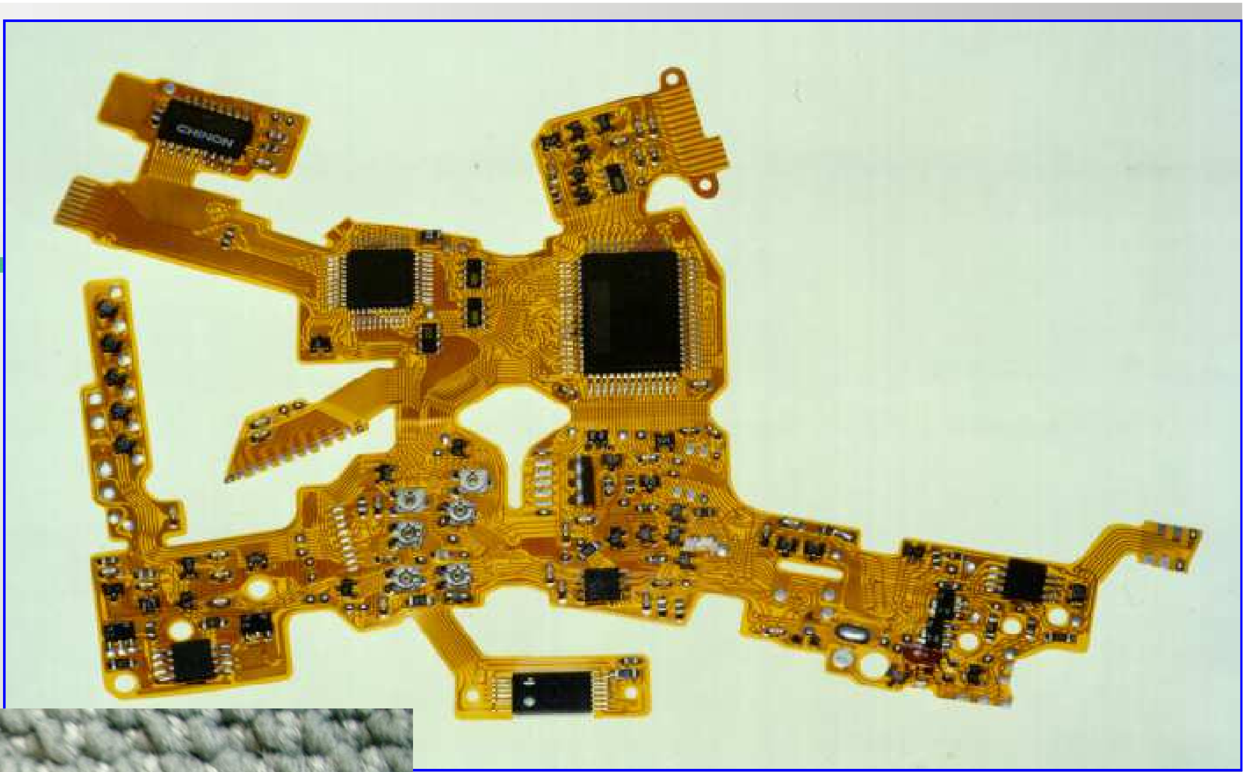






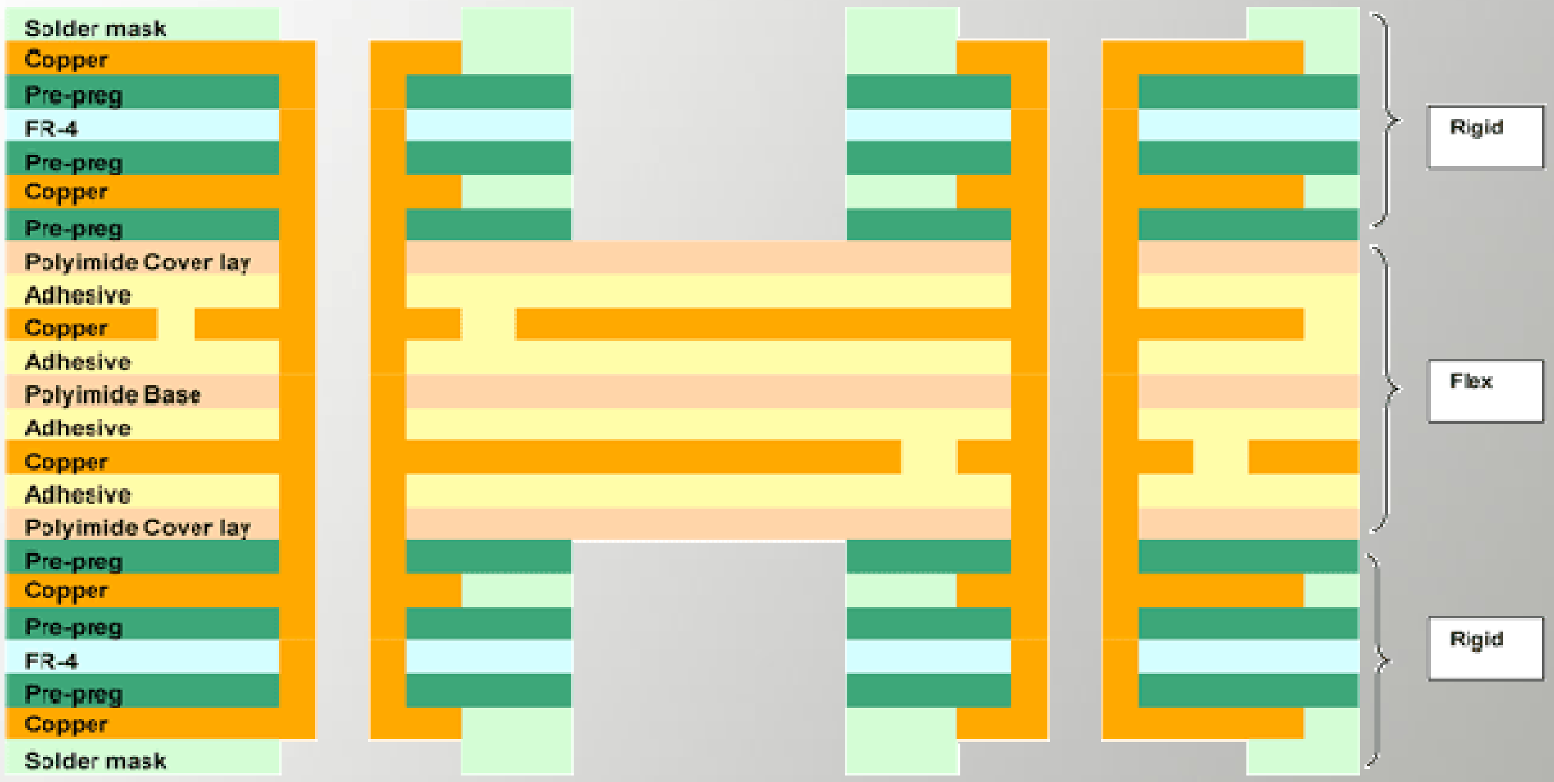


Flexibile PCB



- Flex
- Rigid-flex

Rigid - flex

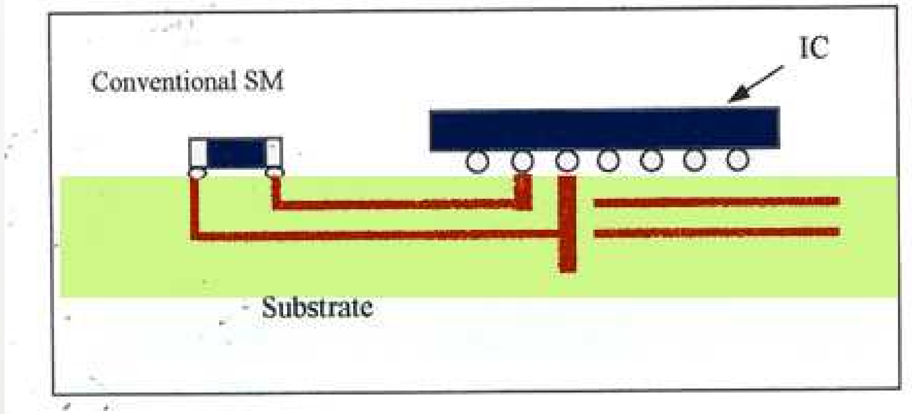


Solder mask
Copper
Pre-preg
FR-4
Pre-preg
Copper
Pre-preg
Polyimide Cover lay
Adhesive
Copper
Adhesive
Polyimide Base
Adhesive
Copper
Adhesive
Polyimide Cover lay
Pre-preg
Copper
Pre-preg
FR-4
Pre-preg
Copper
Solder mask

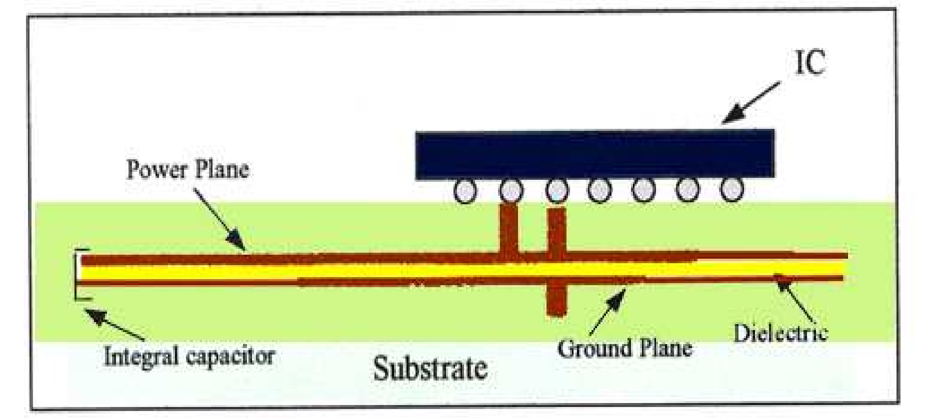
Rigid
Flex
Rigid

Embedded passive parts

Traditional SMT	Embedded passive
Longer wireing	Shorter wireing Reduced size



Conventional surface mounted passive



Embedded capacitor by substitution of dielectric layer

Benefits

- Electrical parameters:
  - Better impedance
  - Shorter signal way, smaller serial inductivity,
  - Minimalize the inductance of the SM parts
  - Reduce cross talking, noise and EMI
- PCB design:
  - Improve density of active elements
  - Less vias, easier wiring
  - Less soldered connections, better reliability
- Economic:
  - Less passive components
  - Improve efficiency of assembly processes
  - Smaller panel size

Barriers

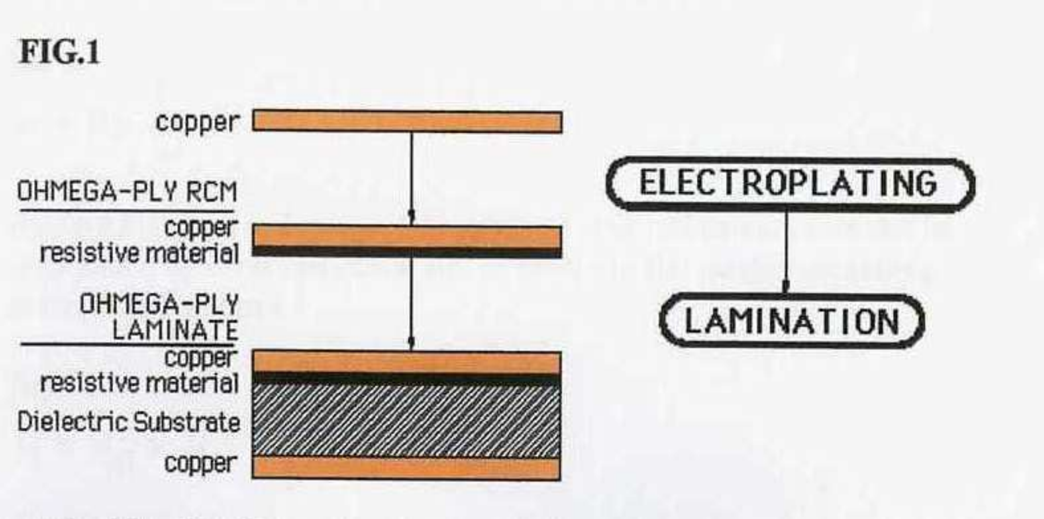
- Only the smaller values of capacitance, resistance and inductance can produce
- The material cost is high
- The manufacturing and the design are more complex

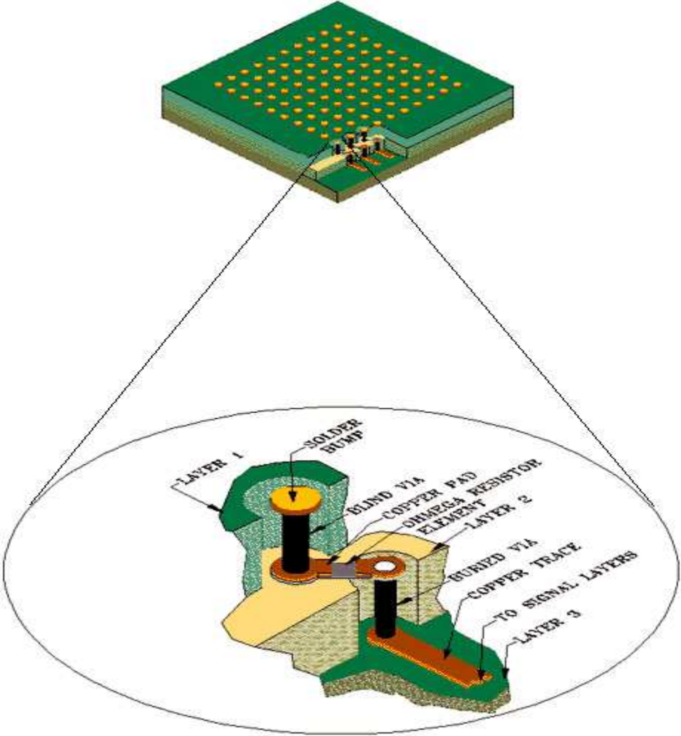
Embeded resistors

- Thin film resistors
- Galvanic plated

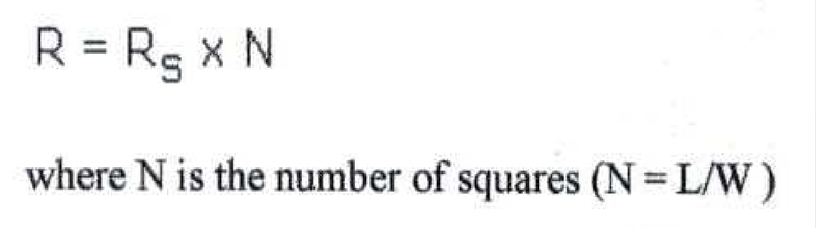
Thick film resistors
Screen printed

FIG.1



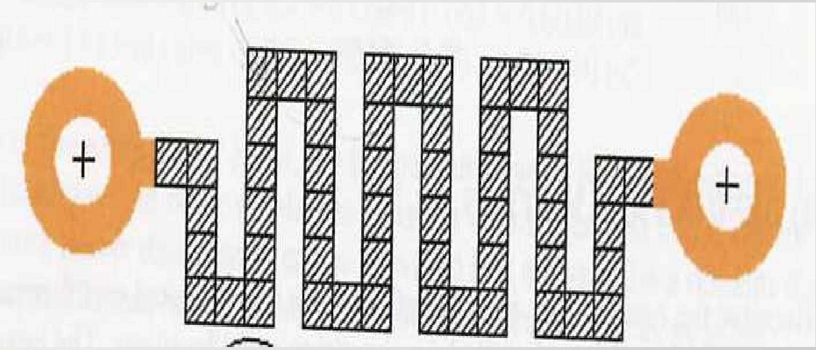


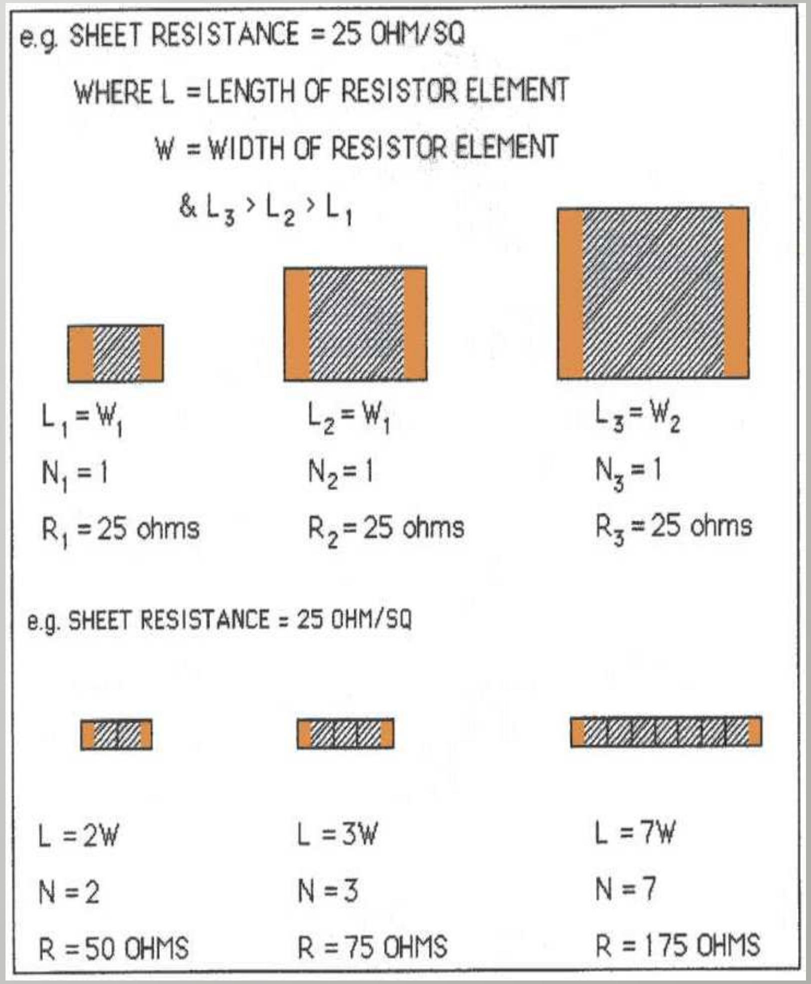
Resistor design (parameters and patterns)



$R = R_S \times N$

where N is the number of squares (N = L/W)





e.g. SHEET RESISTANCE = 25 OHM/SQ

WHERE L = LENGTH OF RESISTOR ELEMENT

W = WIDTH OF RESISTOR ELEMENT

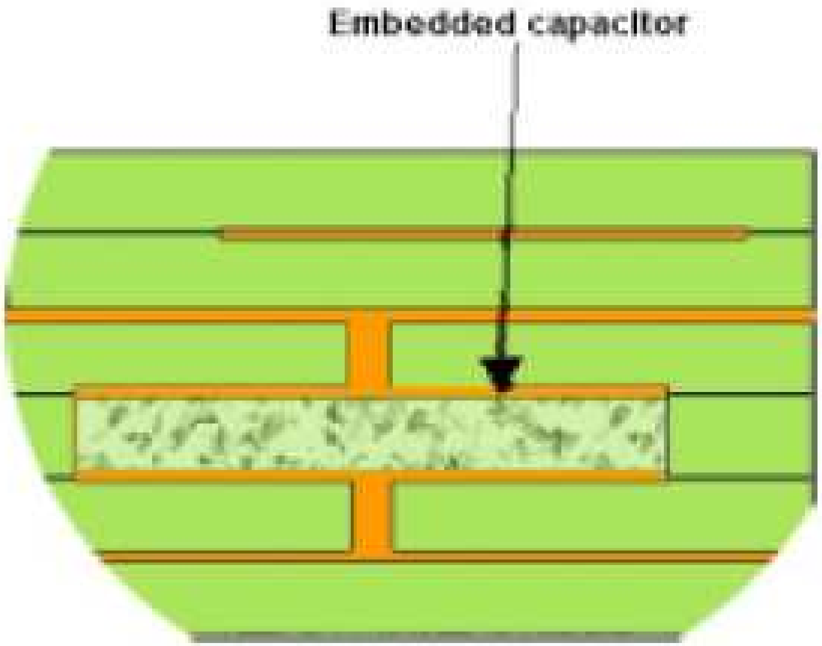
& $L_3 > L_2 > L_1$

$L_1 = W_1$	$L_2 = W_1$	$L_3 = W_2$
$N_1 = 1$	$N_2 = 1$	$N_3 = 1$
$R_1 = 25$ ohms	$R_2 = 25$ ohms	$R_3 = 25$ ohms

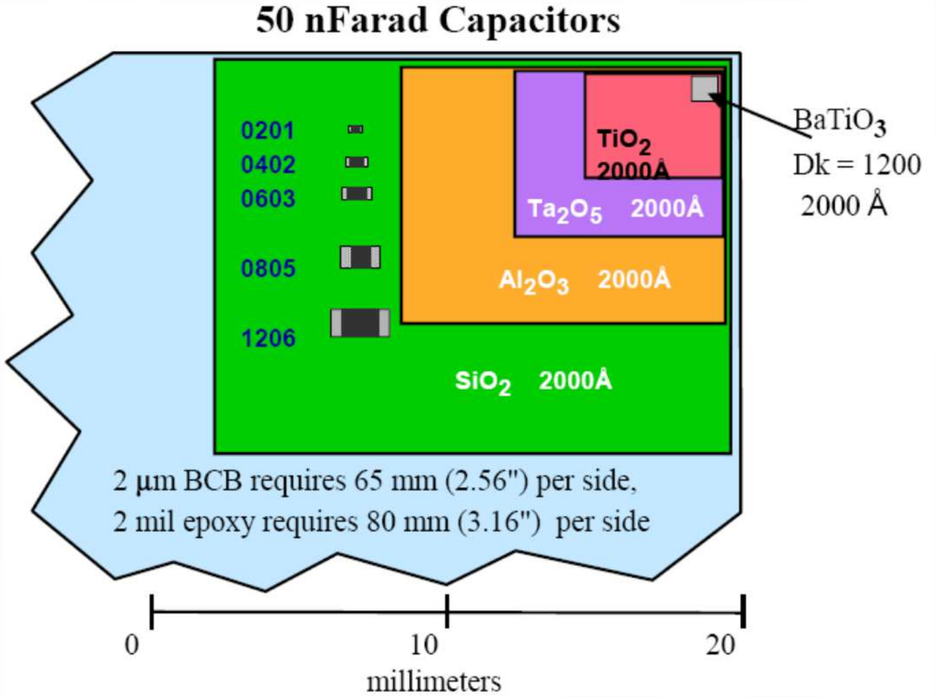
e.g. SHEET RESISTANCE = 25 OHM/SQ

L = 2W	L = 3W	L = 7W
N = 2	N = 3	N = 7
R = 50 OHMS	R = 75 OHMS	R = 175 OHMS

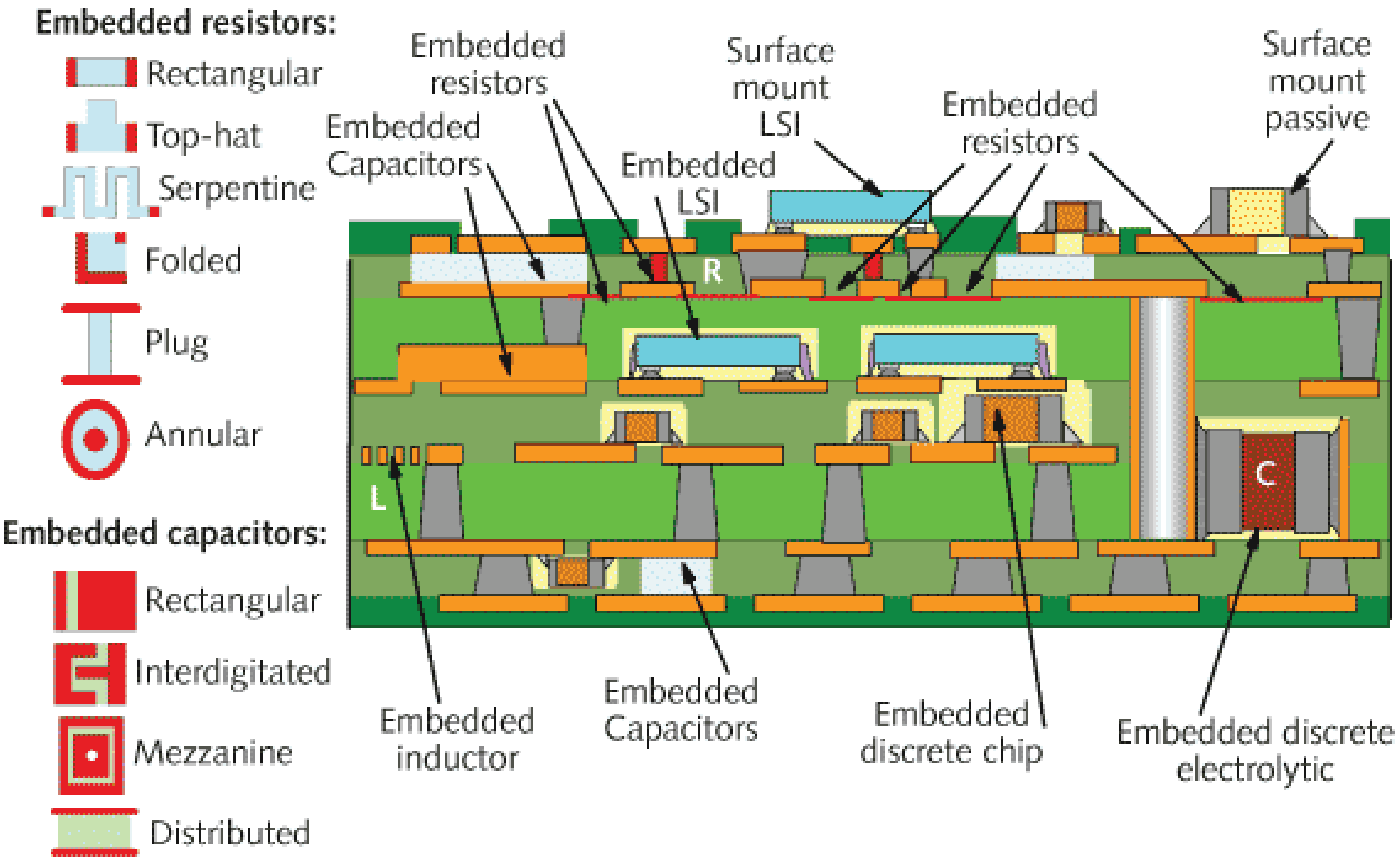
Embedded capacitors

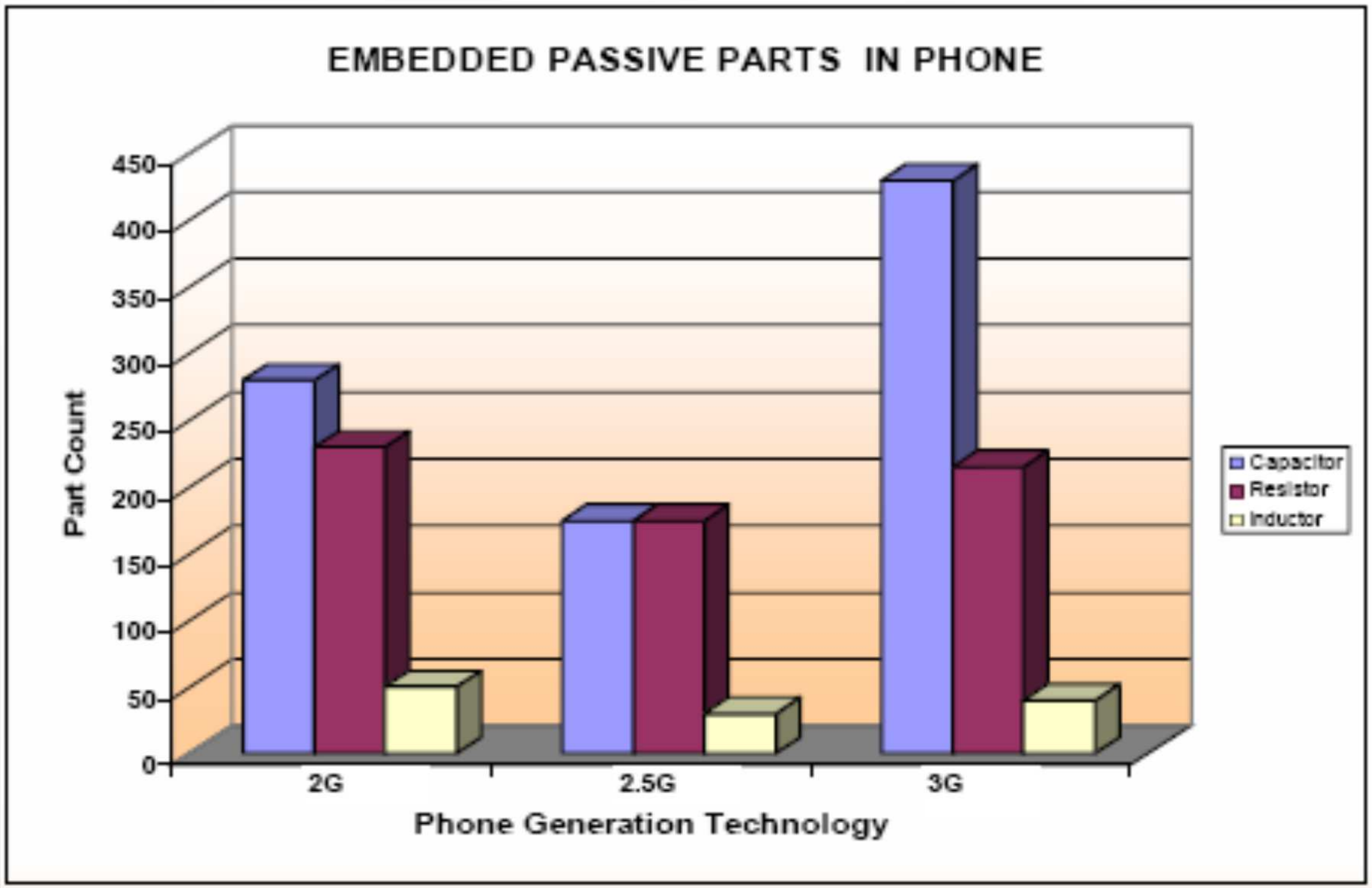


Footprint of a 50 nF capacitor, used different dielectric materials. Thickness is 0,2 μm.



3 D packaging




EMBEDDED PASSIVE PARTS IN PHONE
Part Count
0
50
100
150
200
250
300
350
400
450
2G
2.5G
3G
Phone Generation Technology
Capacitor
Resistor
Inductor