# Introduction to Printed Circuit Board Design For EMC Compliance

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# *Fundamentals of Signal Integrity*

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## ***What is Signal Integrity***

***The ability of electrical signals to travel from a source to load through a dielectric without loss of signal amplitude or parametric values***

In order to solve a signal integrity problem, one must first understand transmission lines and how they function both in theory and reality

***There are two kinds of design engineers:***
***"Those that have signal integrity problems, and those that will"***

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# ***Signal Integrity Concerns***

## It only takes *one* item listed below to cause a signal integrity problem

- Incorrect transmission line routing
- Improper terminations
- Power and/or return plane bounce
- Improper RF return current path
- Mode conversion
- Rise time degradation
- Lossy transmission lines at higher frequencies
- Poor power distribution network
- Hidden parasitics (RLC)
- Propagation delays
- Skin depth and dielectric loss
- Non-monotonic edges
- Excessive inductance in the transmission line
- Excessive ringing and reflection
- Lossy transmission lines
- Poor printed circuit board material
- Overshoot and undershoot
- Impedance discontinuities
- Delta I noise
- RC delay
- Crosstalk
- Stubs and their lengths
- Excessive capacitive loaded lines
- IR drops
- Via stubs
- Excess attenuation
- Non-monotonic edges
- Signal skew
- Gaps in planes
- Dispersion
- Impedance discontinuities
- Unknown parasitic
- Intra line skew
- High dielectric losses

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# ***Aspects of High-Speed Problems***

## Four aspects of high-speed problems are present in system designs

1. **Signal quality:** Reflections and distortions from impedance discontinuities in the signal or return path can affect the quality of the signal. A transmitted signal should see the same impedance throughout all interconnects (includes vias and connectors).
2. **Crosstalk between nets**: Mutual capacitance and inductance exists, both within an ideal and non-ideal return path. One must keep spacing of traces greater than a minimal value while minimizing mutual inductance, keeping the return path impedance as low as possible.
3. **Rail collapse:** A voltage drop within the power and return system when digital components switch logic states. One must minimize the impedance of the power and return path along with the delta-I (current).
4. **EMI:** Can be developed as a result of poor signal integrity within a transmission line. Must minimize bandwidth, ground impedance and common-mode coupling.

Details on impedance discontinuities, transmission line routing, terminations, and simulations are presented later.

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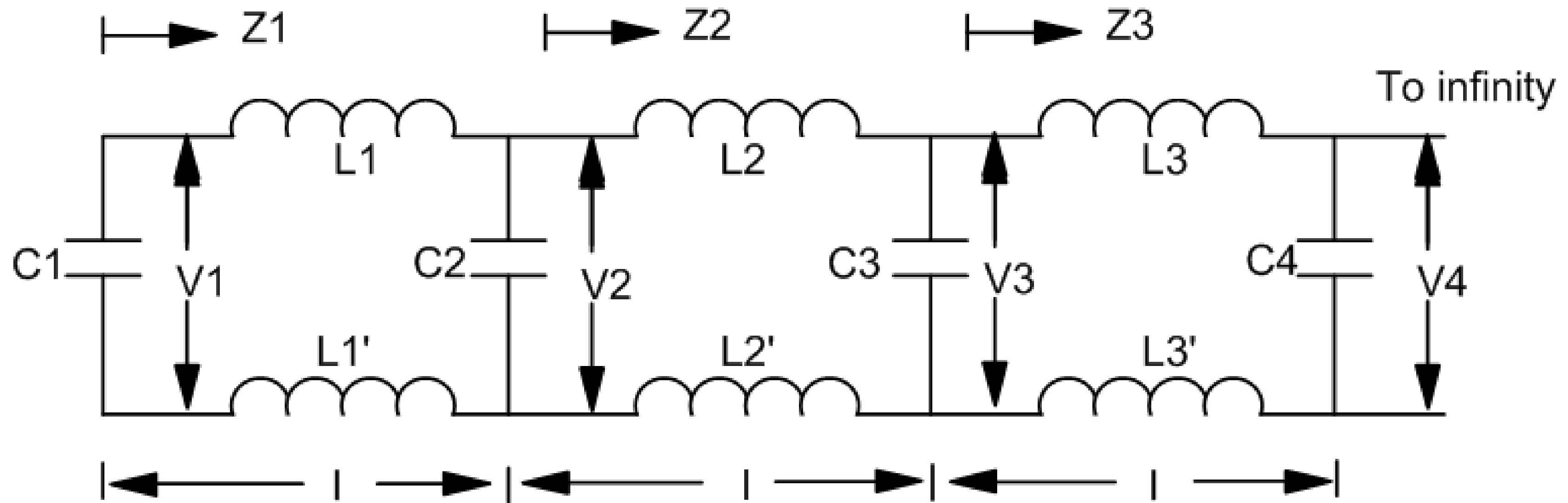
# ***Lossless Transmission Line Equivalent Circuit Within a PCB***




$$Z_o = \sqrt{\frac{L_o}{C_o}} = \frac{V(x)}{I(x)}$$

$$t_{pd} = \sqrt{L_{total} C_{total}}$$

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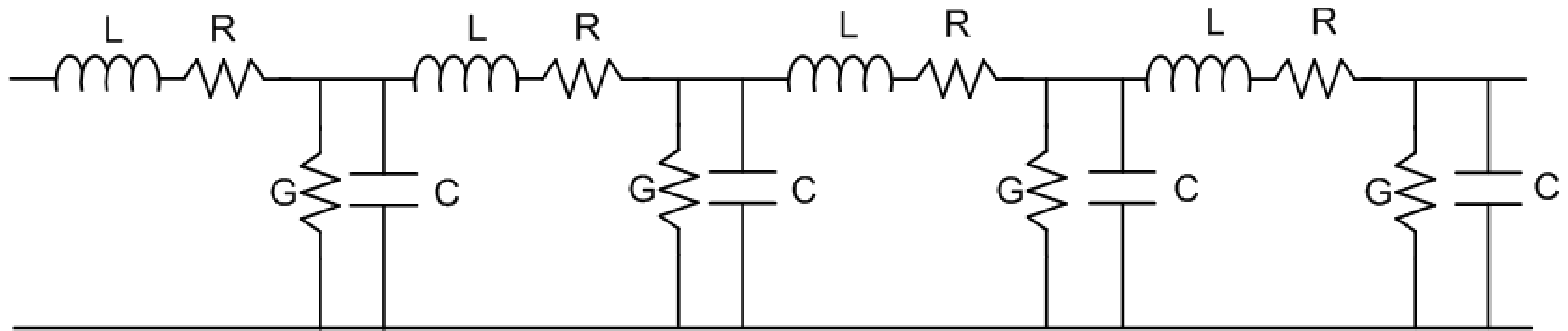
# Lossy Transmission Line Equivalent Circuit Within a PCB




$$V(\omega, x) = V_O \exp(-\Gamma x) \exp(jt)$$

$$\Gamma = \alpha + j\beta = \sqrt{(R_L + j\omega L_L) + (G_L + j\omega C_L)}$$

$$Z_O = \sqrt{\frac{(R_L + j\omega L_L)}{(G_L + j\omega C_L)}}$$

$Z_O =$ *characteristic impedance*

$L =$ *line length*

$R_L, G_L$ *may vary with frequency*

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# *Lossy Transmission Lines*

1. **Resistive losses** - Constant with frequency. Attenuation, usually measured in dB/unit distance, is proportional to the resistance per unit length of the conductor.

2. **Skin effect losses** - Proportional to the square root of frequency. As signal frequency increases, current flow retreats to the surface of the conductor flowing in a "skin" which becomes thinner with increasing frequency. Resistivity of the material stays the same, it is the cross section that decreases related to AC current flow.

3. **Dielectric losses** - The PCB material (core and prepreg) absorbs some of the electric field energy, which is directly proportional to frequency. Dielectric loss or dissipation factor (magnitude of energy loss) is not the same as dielectric constant (speed of signal travel).

4. **Resonances** - Typically caused by improperly terminated traces and split planes in addition to the lumped magnitude of both capacitance and inductance within power distribution networks.

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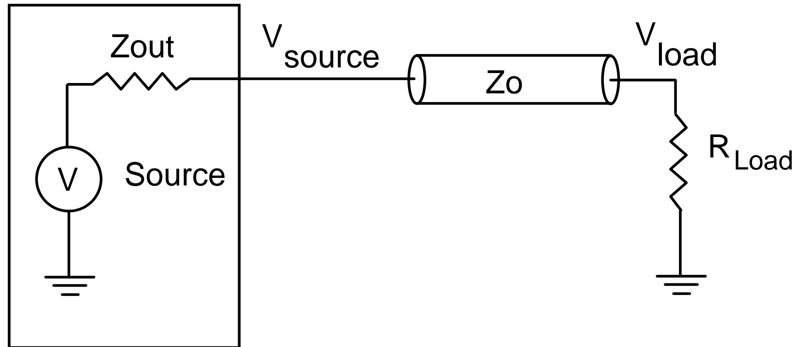
# Typical Transmission Line System

- Minimum reflections will occur when $Z_{out} = Z_o$ *and* $Z_o = Z_{load}$
- Maximum energy transfer occurs when $Z_{out} = Z_o = Z_{load}$




RG174 - 50 Ω
RG58 - 50 Ω
RG59 - 75 Ω
RG62 - 93 Ω
TV Antenna - 300 Ω
Cable TV - 75 Ω
Twisted pairs - 70-120 Ω

If the load is not matched, a voltage is reflected back toward the source. The value of reflected voltage ($V_r$) and the percentage of the propagation signal reflected back towards the source (%) is:

$$V_r = V_o\left(\frac{R_{Load} - Z_o}{R_{Load} + Z_o}\right) \qquad \%\ reflection = \left(\frac{Z_L - Z_o}{Z_L + Z_o}\right) \times 100$$

where $V_r$ = reflected voltage
$V_o$ = source voltage
$R_L$ = load resistance
$Z_o$ = characteristic impedance of the transmission path

When $R_L$ is less than $Z_o$, a negative reflected wave exist. If $R_L$ is greater than $Z_o$, a positive wave is observed. This reflected wave will bounce back and forth between source and driver until dielectric losses absorbs the signal.

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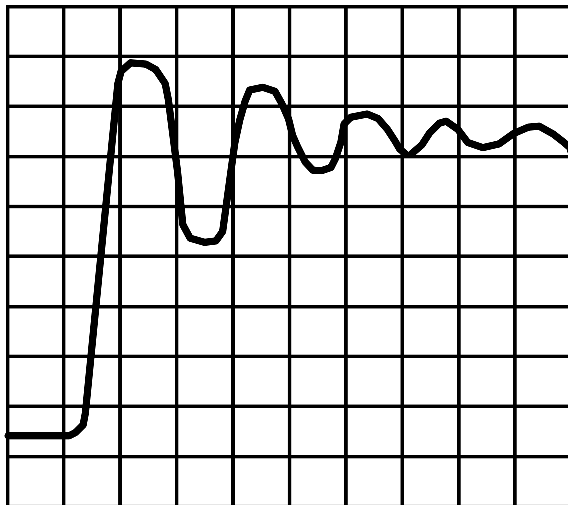
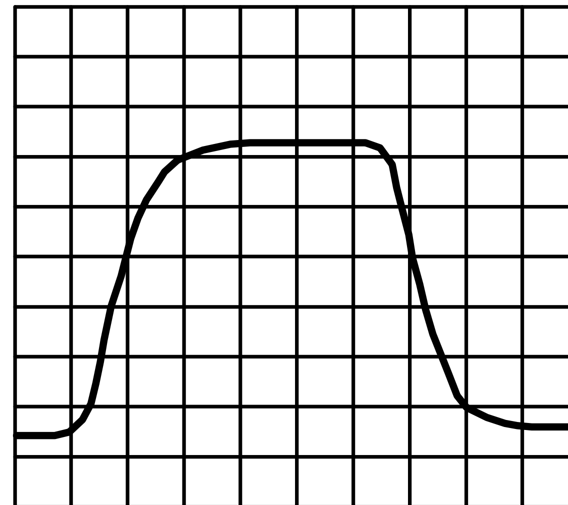
## ***Reflections – Poor Signal Integrity***

Reflections will occur within a transmission line if not properly terminated. The following causes reflections.

- Changes in trace width
- Improperly matched termination networks
- Lack of terminations
- T-stubs, branched or bifurcated traces
- Varying loads and logic families
- Connector transitions
- Any changes in impedance of the transmission line routing



Ringing indicates reflections (excessive inductance)



Rounding indicates excessive capacitance

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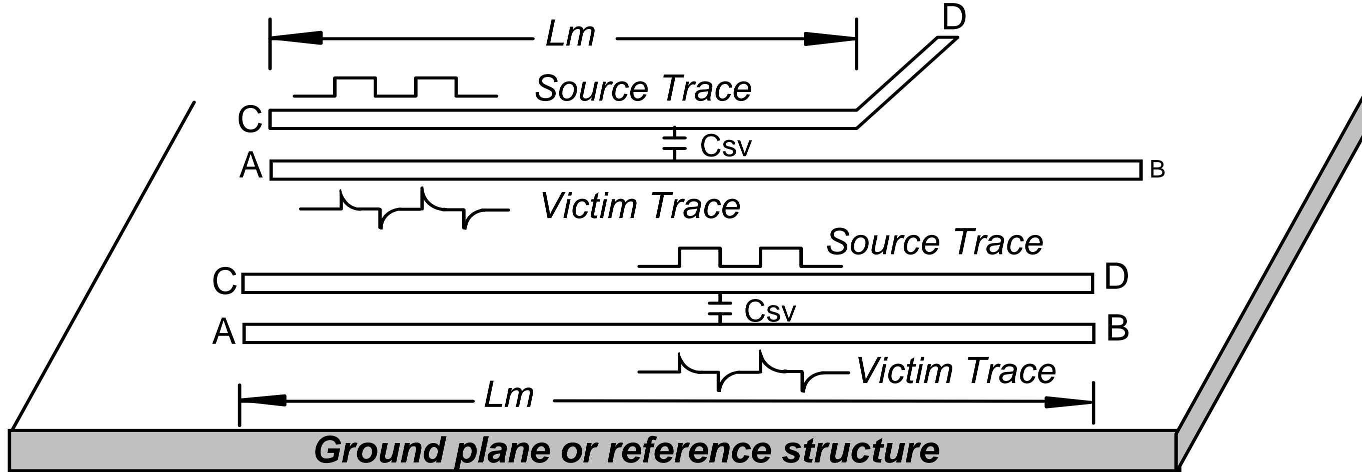
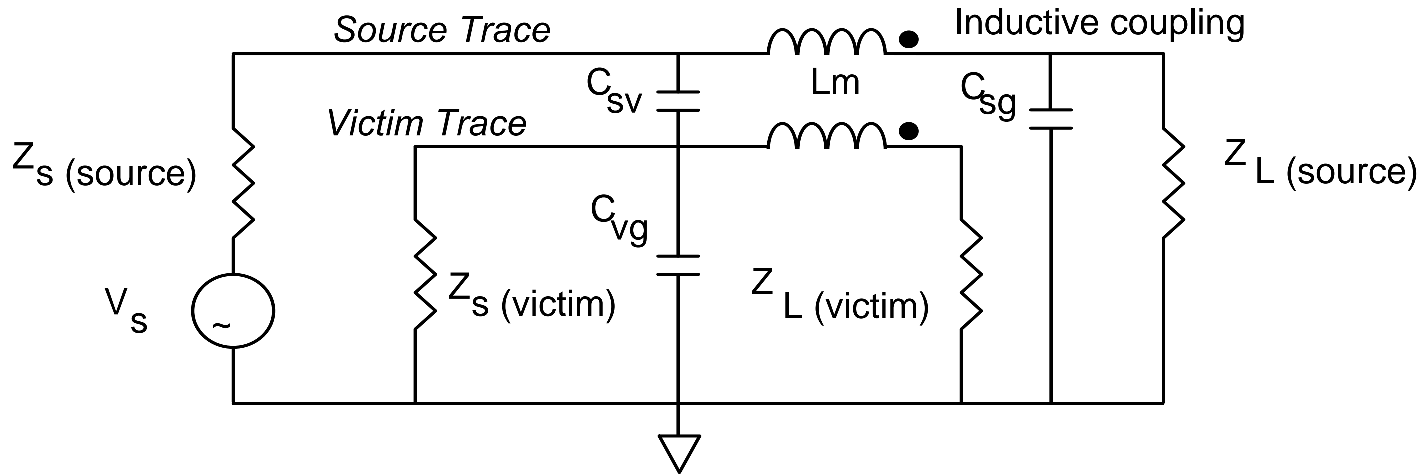
# Crosstalk – Fundamental Aspects of Coupling




$$Z_V = \frac{Z_S (v) \times Z_L (v)}{Z_S (v) + Z_L (v)}$$

$C_{sv}$ = Capacitance between source trace and victim trace

$C_{vg}$ = Capacitance between victim trace and ground

$C_{sg}$ = Capacitance between source trace and ground

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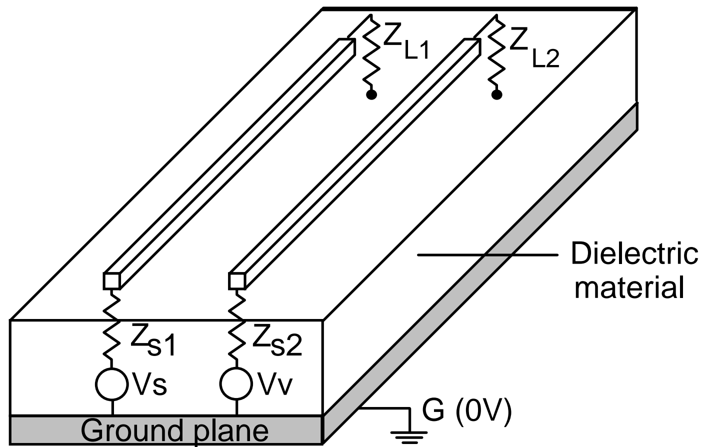
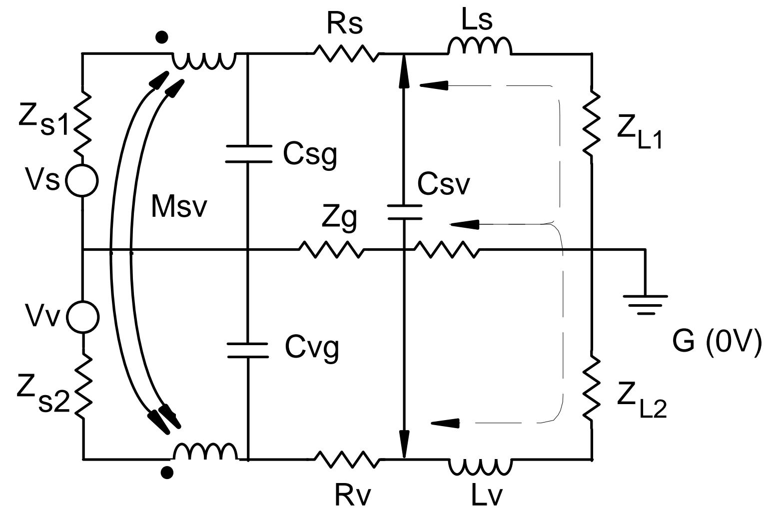
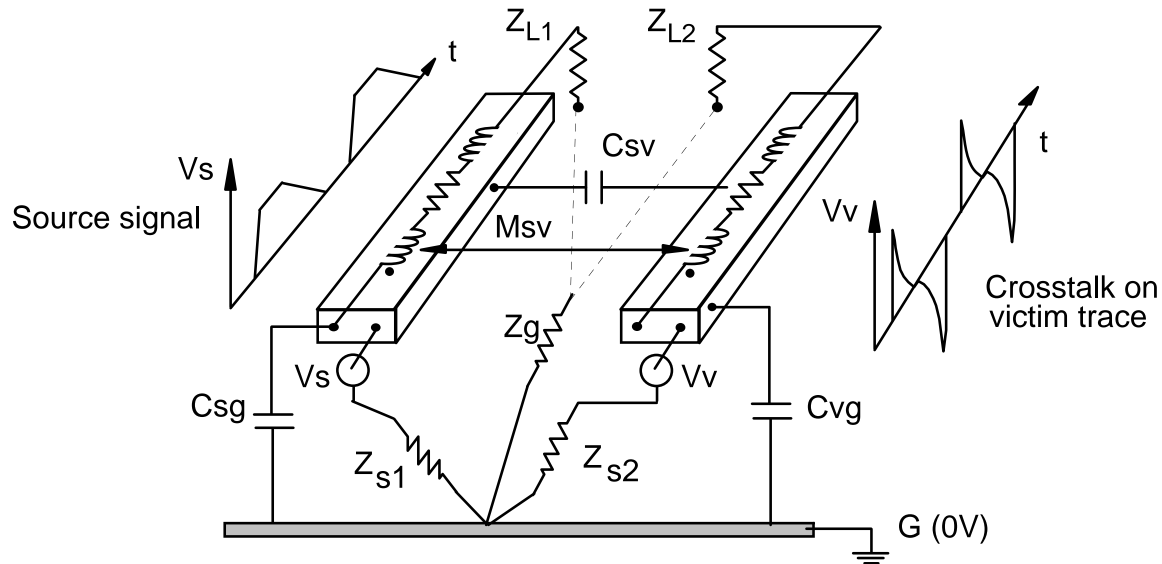



Parallel traces over a ground plane




Schematic representation of a three wire circuit

$C_{sv}$ = Capacitance between source trace and victim trace
$C_{vg}$ = Capacitance between victim trace and ground
$C_{sg}$ = Capacitance between source trace and ground

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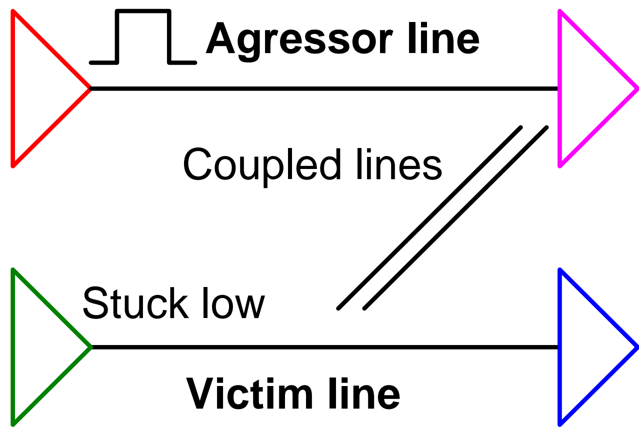


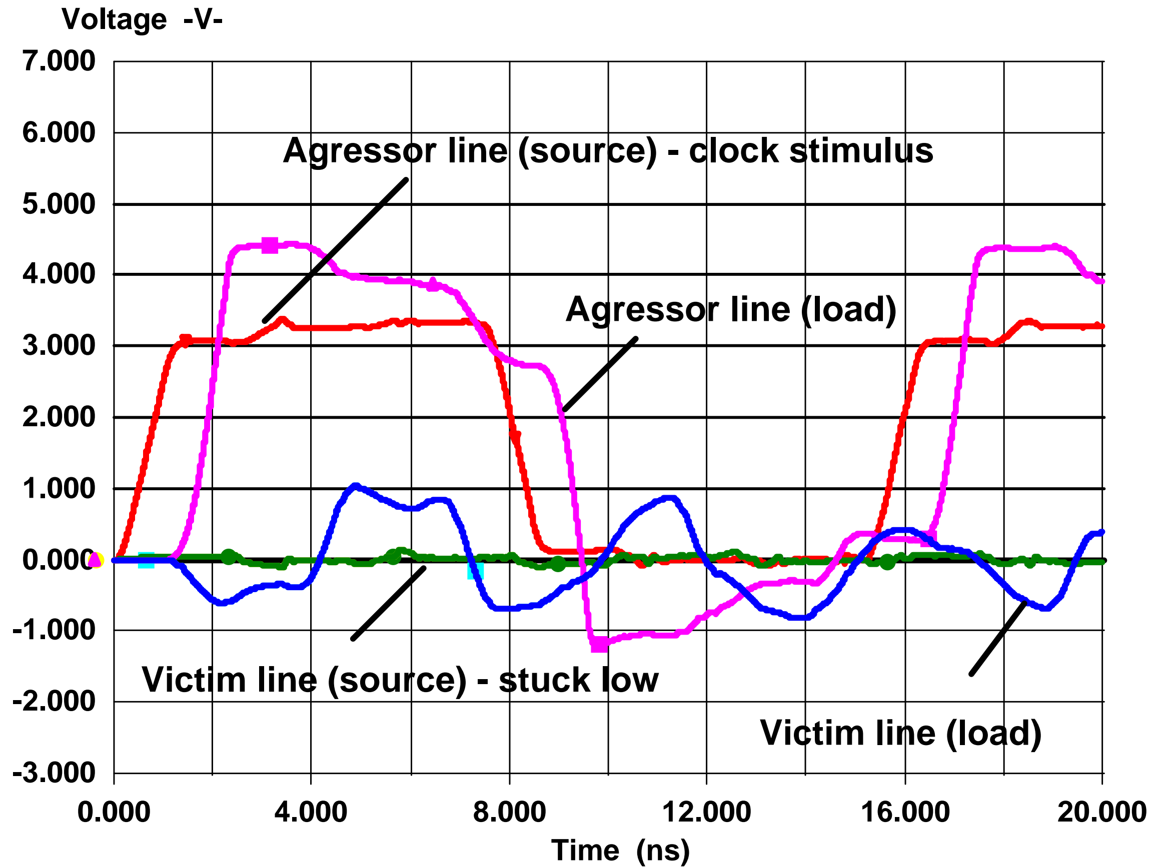


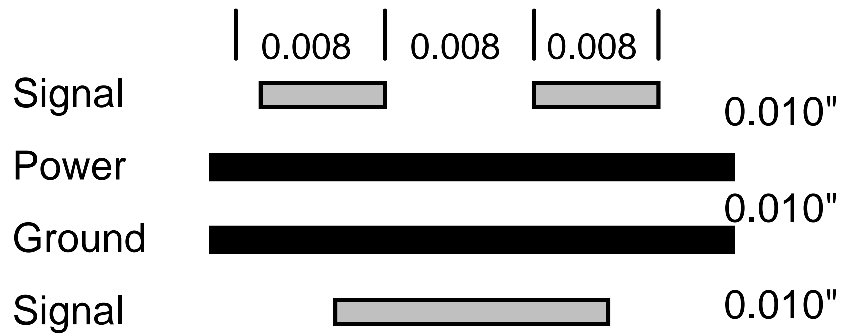


8.0 inches (20.3 cm) long, 72.1 ohms

Propagational delay: 1.126 ns

Oscillator: 66 MHz, 49% duty cycle

CMOS, 3.3V, Fast

Traces: 0.008" wide and 0.008" apart (.20mm)

Distance to reference plane: 0.010" (.25mm)

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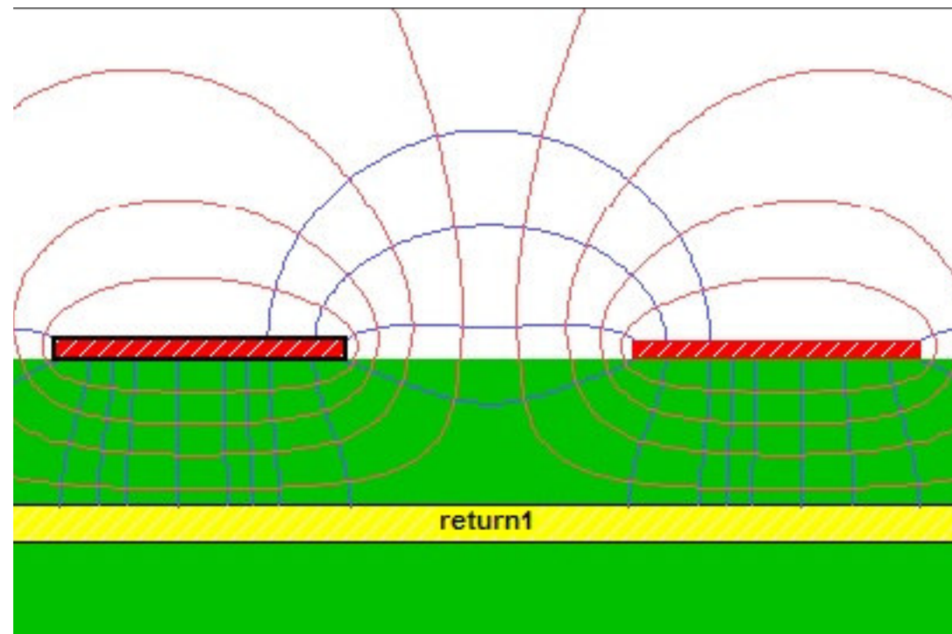
## *Common Forms of Crosstalk*

### Far End Cross Talk

Only appears in surface traces and scales with coupling length, inversely with rise time and depends on line to line spacing. Reduce it by shorter coupling lengths, longer rise time, larger spacing, or best of all, route in stripline.

### Near End Cross Talk

Saturates with coupling length when coupling TD > ½ RT (rise time), predominantly affected by line to line spacing and can be reduced with lower dielectric constant.

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## ***Sample List of Design Techniques to Prevent Crosstalk***

To prevent crosstalk within a PCB, the following design and layout techniques are useful.

- Crosstalk will increase with a wider trace width as mutual capacitance, *Cm*, increases.
- With long parallel traces, greater mutual inductance, *Lm*, is present.
- Crosstalk also increases with faster edge rates and frequency of operation.

1. Group logic devices according to functionality.
2. Minimize routed distance between components.
3. Minimize parallel routed trace lengths.
4. Locate components away from I/O interconnects and areas susceptible to field corruption.
5. Provide terminations for traces rich in harmonic energy.
6. Avoid routing of traces parallel to each other with adequate separation between the tracks.
7. Route adjacent signal layers (either microstrip or stripline) orthogonally to prevents capacitive and inductive coupling between two planes in parallel.
8. Reduce signal-to-ground reference distance separation.
9. Reduce trace impedance and/or signal drive level.
10. Isolate signal layers routed in the same axis by a solid planar (typical of backplane designs).

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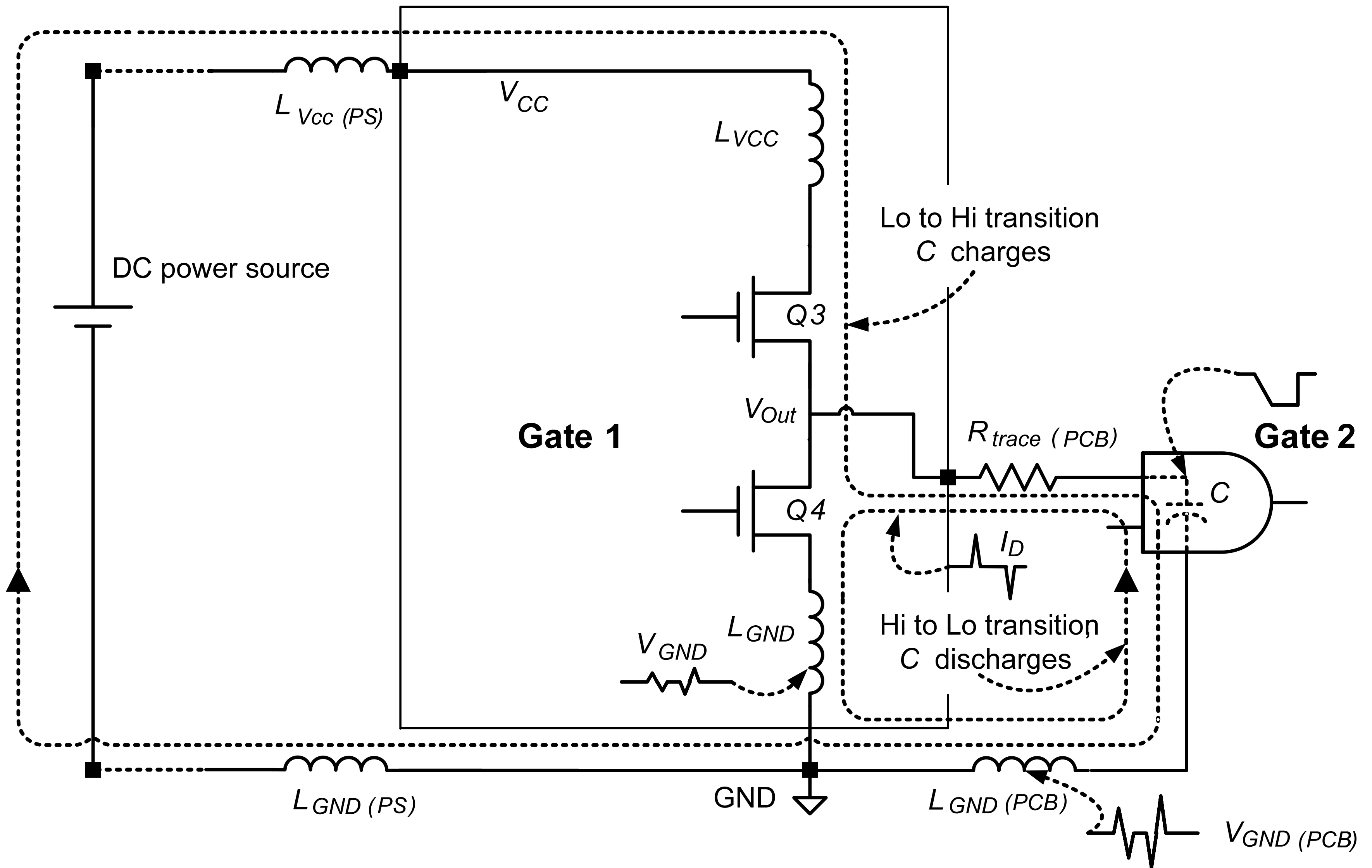
# Power and/or Return Plane Bounce

$$V_{power/return} = L_{power/return} \frac{dI_{discharge}}{dt}$$

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# *Fundamentals of EMC*

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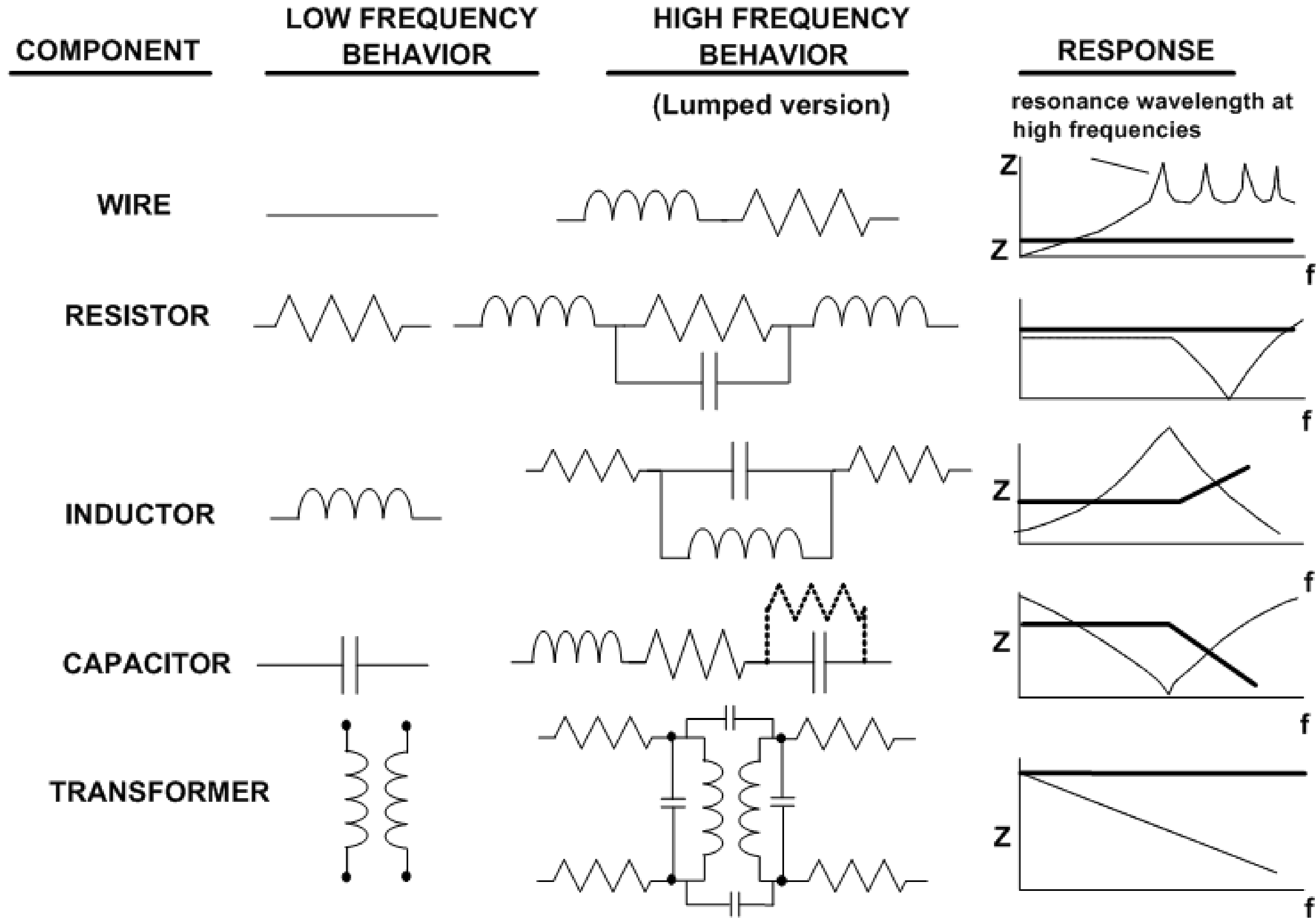
# Component Characteristics at RF Frequencies

**(The Hidden Schematic)**




**Response curves**
Solid line is low frequency behavior
Dashed line is high frequency behavior

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## ***How RF Energy is Created – Maxwell Made Simple***

Maxwell's four equations describe the relationship of electric and magnetic fields. Equations are derived from:

- Ampere's Law
- Faraday's Law
- Two from Gauss's Law.

**To overly simplify Maxwell, use Ohms law**

**Ohms Law (time domain-DC currents)**

$$V = I\,R$$

**Ohms Law (frequency domain-AC currents)**

$$V_{rf} = I_{rf}\,Z$$

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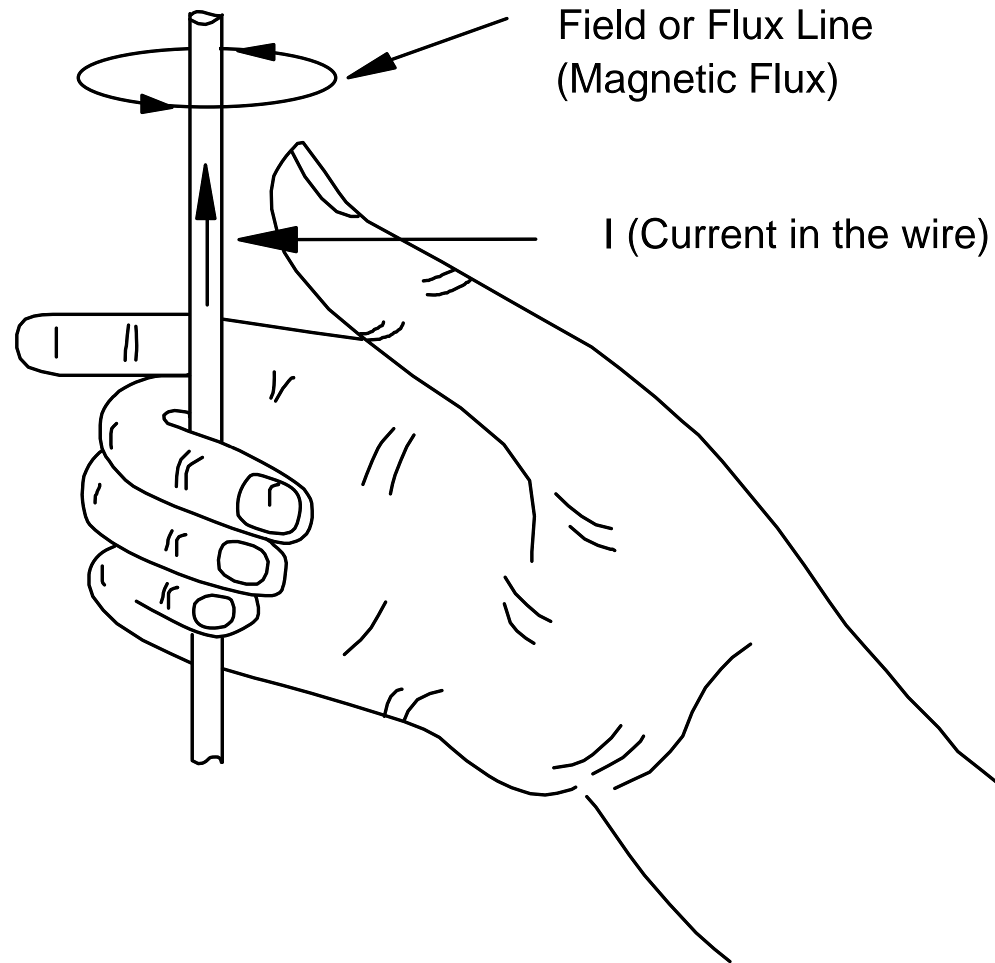
# ***Right Hand Rule***

## *(Faraday's Law)*




Where is the electric field? In the direction of current flow.
Only the magnetic field is shown as a flux line.

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# Maxwell's Equations

**(For Reference Purposes)**

*First Law : Electric Flux (from Gauss)*

$$\nabla \bullet D = \rho \qquad \varphi_e = \oint_s D \bullet ds = \int_v \rho \, dv = 0$$

*Second Law : Magnetic Flux (from Gauss)*

$$\nabla \bullet B = 0 \qquad \varphi_m = \oint_s B \bullet ds = 0$$

*Third Law : Electric Potential (from Faraday)*

$$\nabla \times E = -\frac{\partial B}{\partial t} \qquad \oint E \bullet dl = -\int_s \frac{\partial B}{\partial t} \bullet ds$$

*Fourth Law : Electric Current (from Ampere)*

$$\nabla \times H = J + \frac{\partial D}{\partial t} \qquad \oint H \bullet dl = \int_s \left( J + \frac{\partial D}{\partial t} \right) \bullet ds = I_{total}$$

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# ***Electric and Magnetic Field Impedance***

A plane wave is a combination of both electric and magnetic field components (Poynting vector). Fields propagate from a field source near the velocity of light.

$$c = 1/\sqrt{\mu_o \varepsilon_o} = 3 \times 10^8$$

where $\mu_o = 4\pi * 10^{-7}$ H/m
$\varepsilon_o = 8.85 * 10^{-12}$ F/m

**Electric field component is measured in volts/meter (Note-voltage)**
**Magnetic field component is in amps/meter (Note-current)**

The ratio of both electric field (E) to magnetic field (H) is identified as the "impedance" of free space. This impedance ratio is described by:

$$Z_o = E \times H = \sqrt{\mu_o / \varepsilon_o} = 377 \text{ ohms}$$ **(Note-resistance)**

Energy carried in the wave front is measured in Watts/meter$^2$ **(Note-power)**

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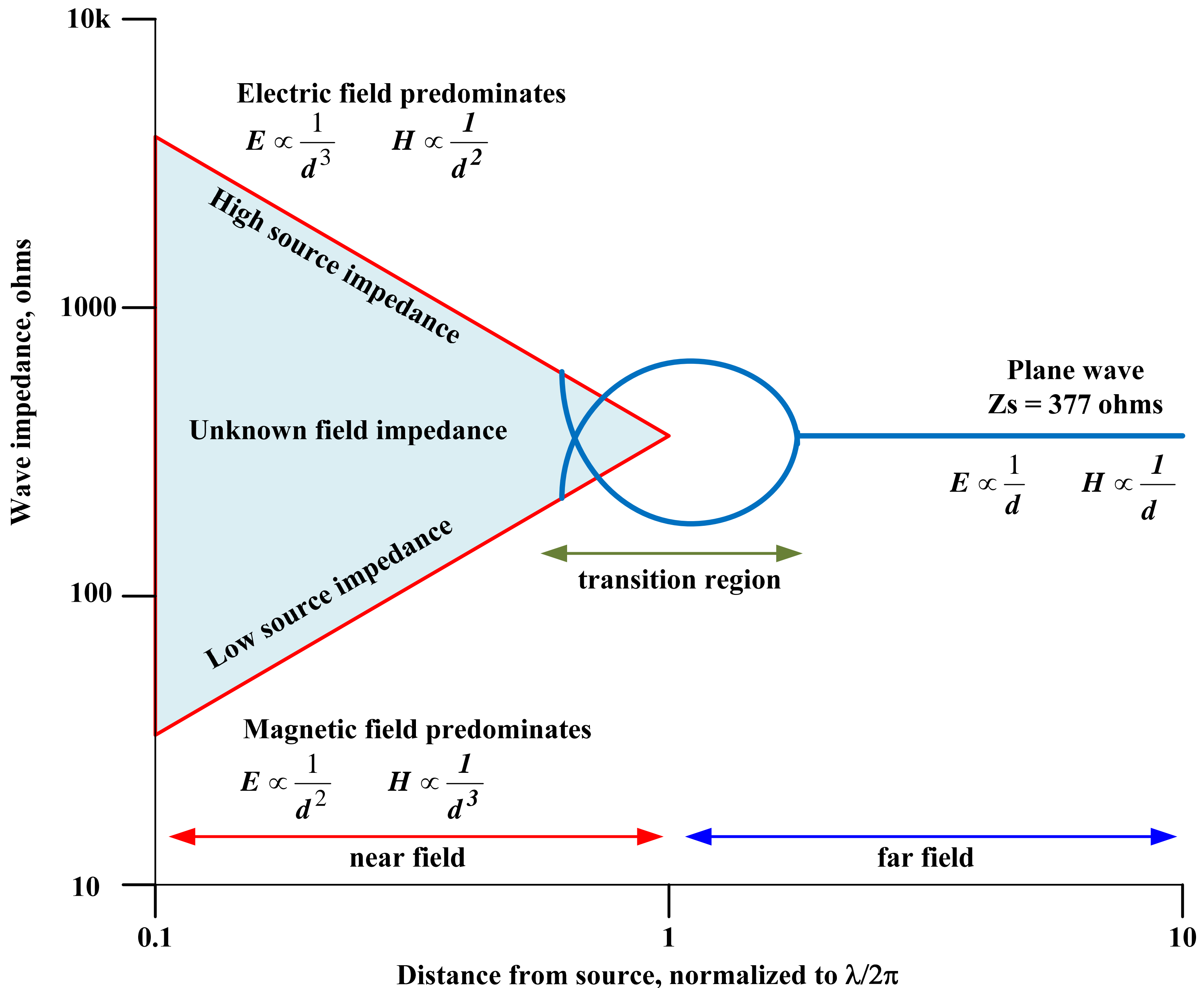


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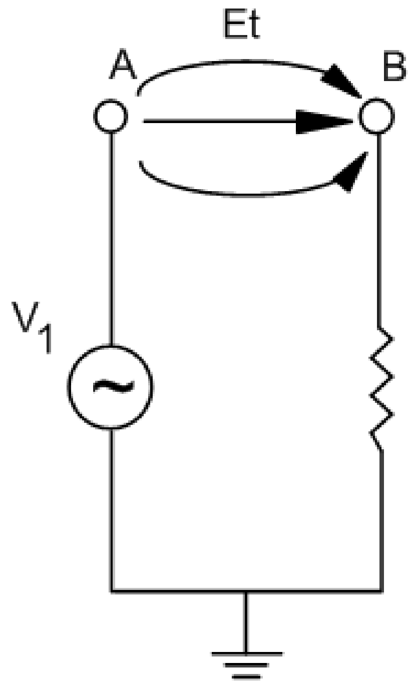
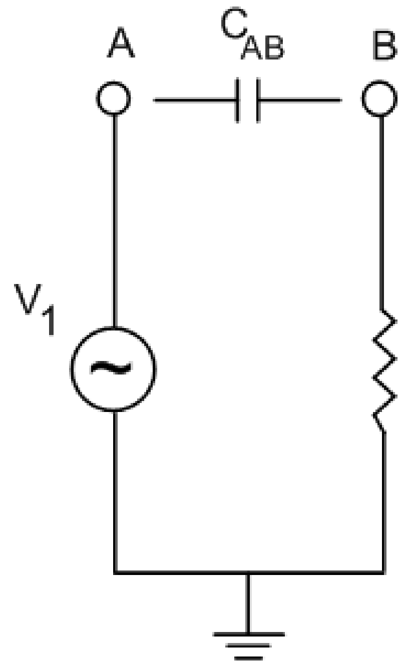
# *Electric and Magnetic Field Representation*

**Electric Field**

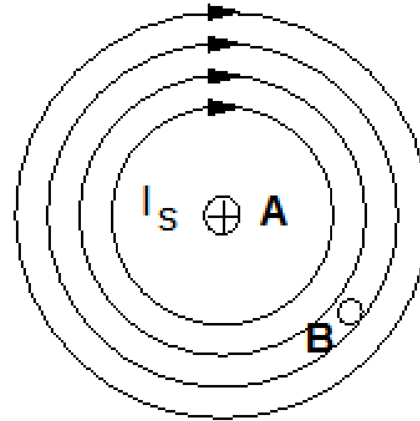


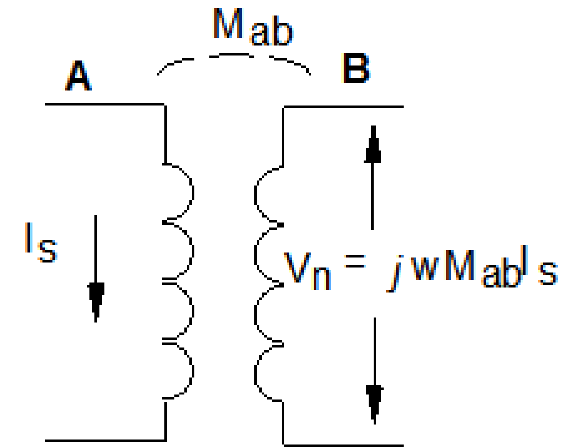




Physical Representation   Equivalent Circuit

**Dipole Antenna**

**Magnetic Field**




Physical Representation   Equivalent Circuit

**Loop Antenna**

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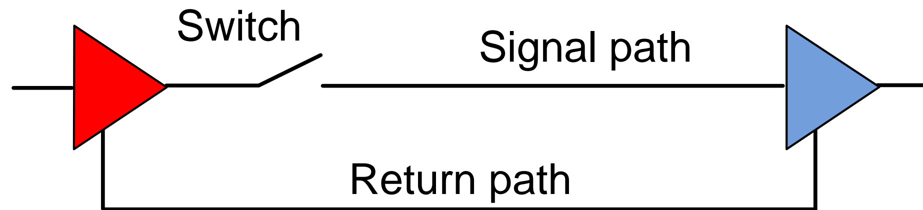
## ***Closed Loop Circuit***




If a continuous, conductive low impedance RF return path is not present (transmission line impedance is greater than 377 ohms), the return path will be free space (377 $\Omega$ at $\lambda/4$), which may be much less than the impedance of a localized RF return path.

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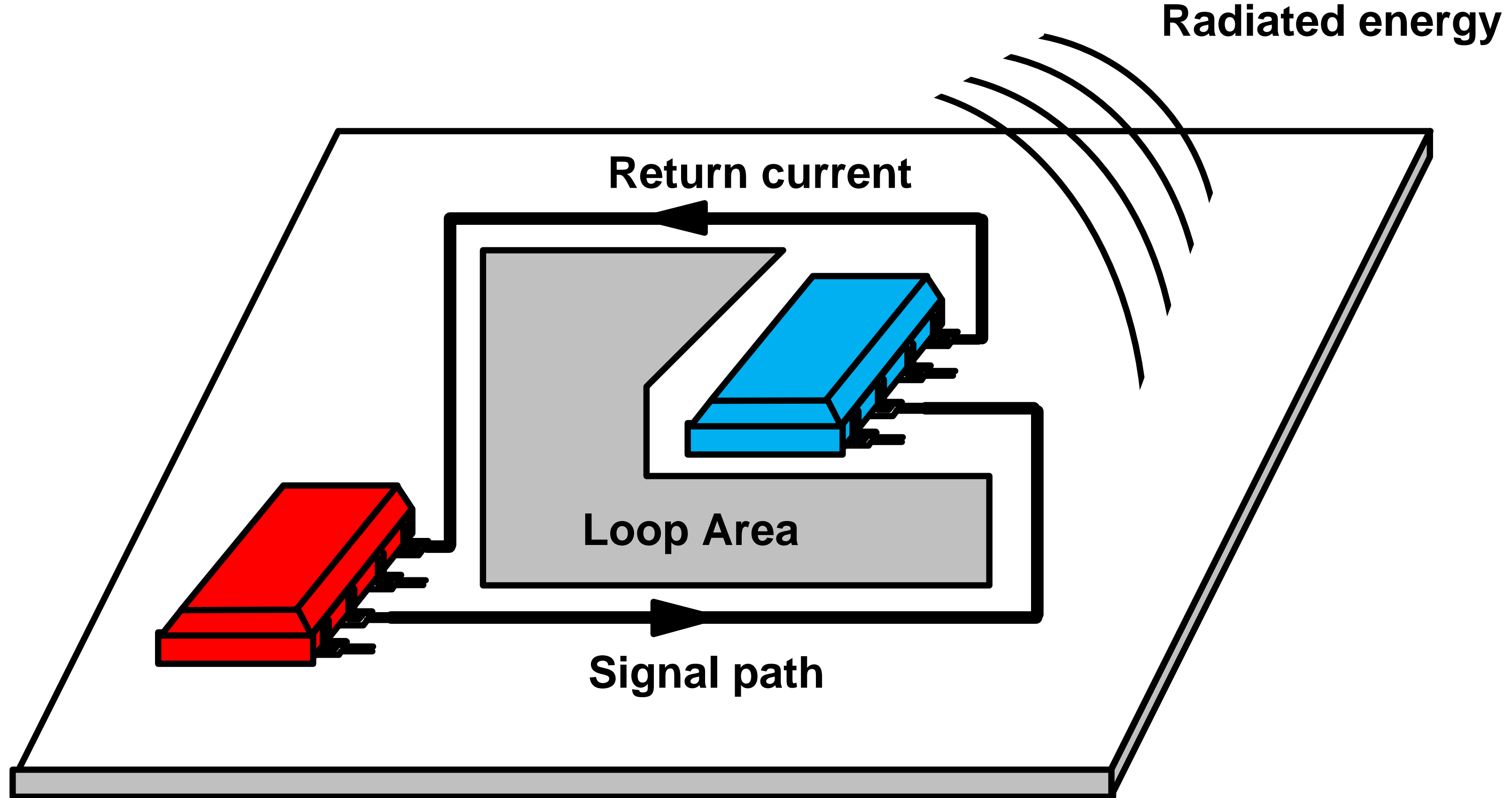
# ***Radiated Emissions from a Closed Loop Circuit***




This configuration is for a single- or double-sided PCB.

For a multi-layer PCB, loop area is in the plane directly below the signal path.

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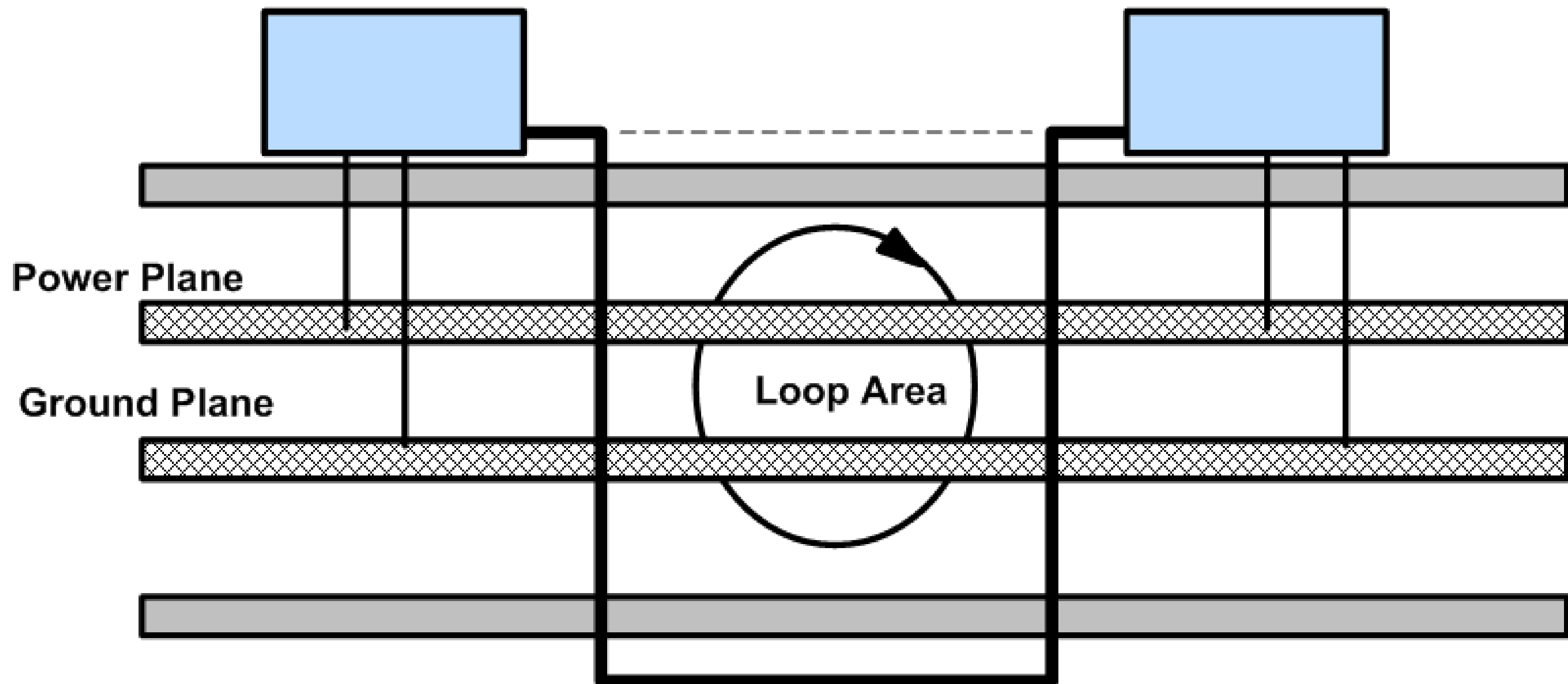
# Loop Area Between Circuits or Components – Different Layers




The real loop area is longer than shown, as the transmission line must have both a source and return path. Only the source path is shown. The return path is through either the power or ground plane, depending on application.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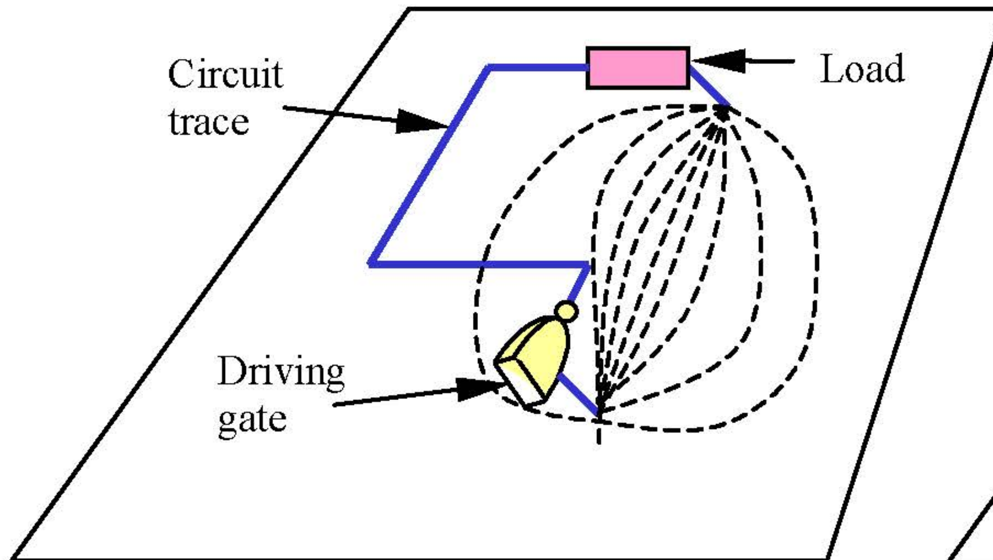
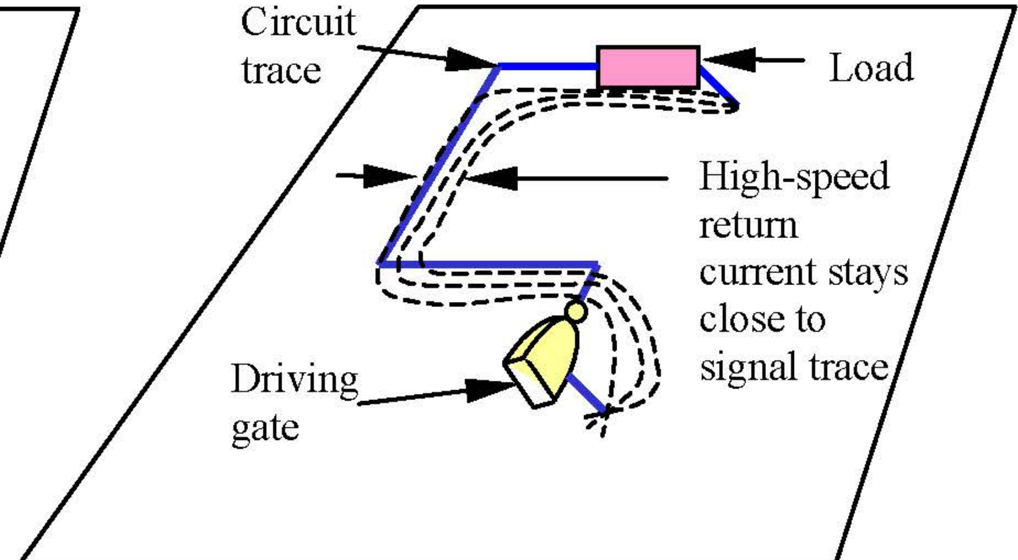
## *Return Current Path of Travel – Multilayer Assembly*

**Low frequency operation**

**High frequency operation**




a) At low frequencies current follows the path of least resistance




b) At high-frequencies current follows the path of least inductance

Illustration provided courtesy: Dr. Howard Johnson

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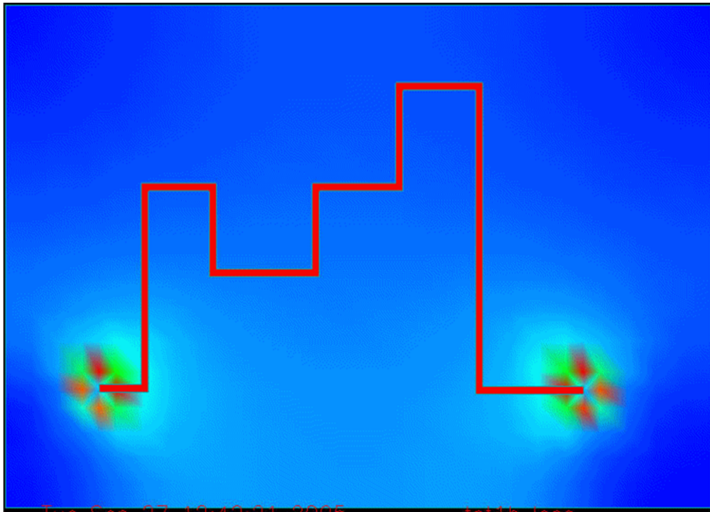
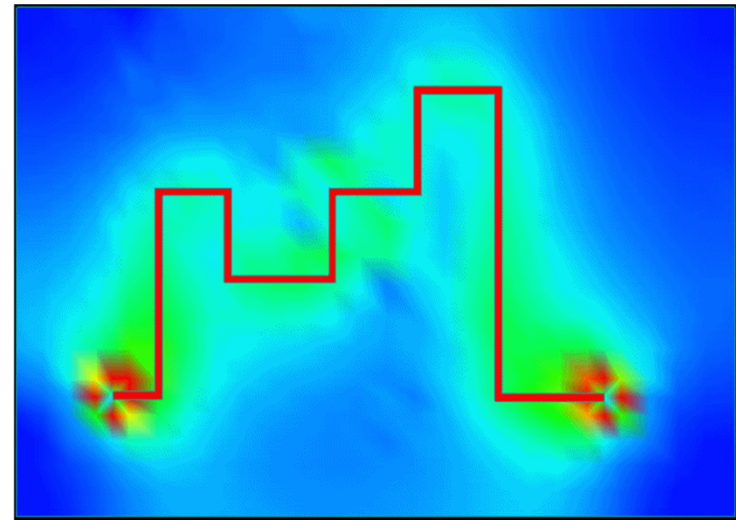
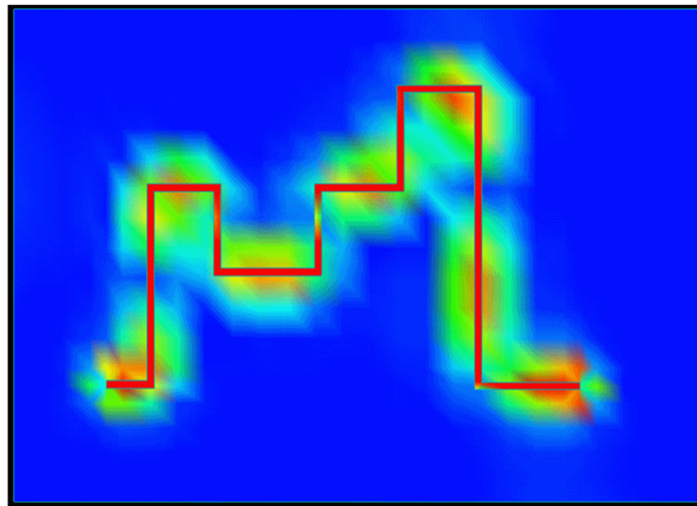


Circuit Return Current Simulation @ F=1 Hz



Circuit Return Current Simulation @ F=100 kHz



Circuit Return Current Simulation @ F=5 GHz

Courtesy of Alexander Perez, Agilent Technologies

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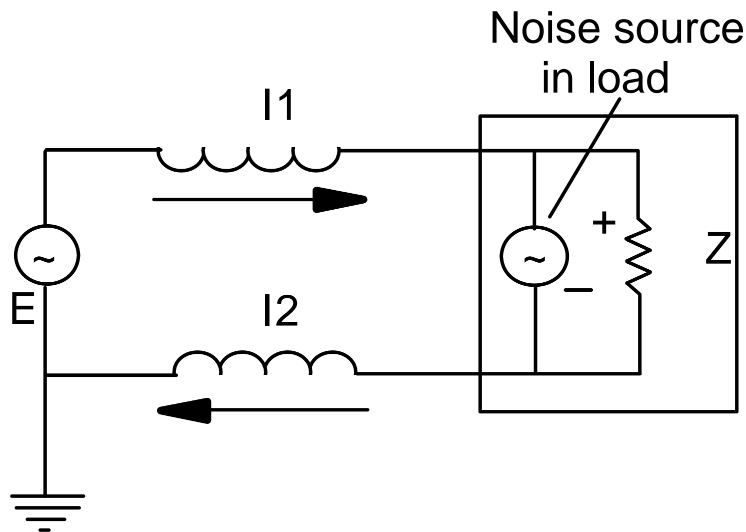
# ***Common-Mode and Differential-Mode Currents***

**Differential-mode**

1. Conveys desired information.
2. Does not cause interference as the fields generated oppose each other and cancel out.

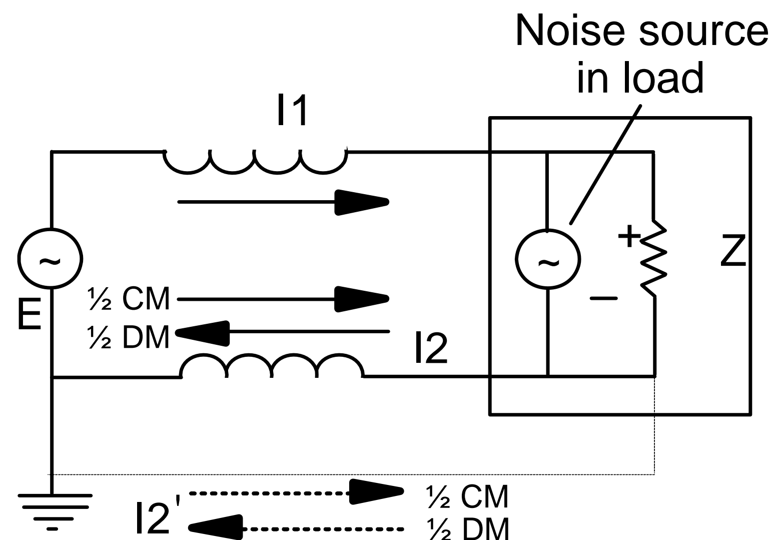
**Common-mode**

1. The major source of cable radiation.
2. Contains no useful information.
3. Has no useful purpose.
4. Causes a system (traces, cables, etc.) to radiate as a monopole antenna.




**Differential-mode current**

$$I\,total = \frac{I1 - I2}{2}$$




**Common-mode current**

$$I\,total = \frac{I1 + I2}{2}$$

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## ***Summary on How EMI Is Developed Within the PCB***

1. Current transients are created by the production of high frequency periodic signals injected into the power and return distribution network.
2. An RF voltage drop develops across any impedance within a transmission line.
3. Common-mode RF currents are created by this RF voltage drop on unbalanced RF current return path.
4. Radiated emissions, created by these common-mode RF currents, are observed on internal antenna structures by virtue of poor RF ground loop or return path control.
5. When any time-variant current is injected into a trace, magnetic flux is developed, which in turn creates an electric field. The combination of electric and magnetic fields create a propagating plane wave.
6. Lack of a proper RF current return path exacerbates EMI.

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# *Basic EMC Suppression and Grounding Concepts*

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## ***Different Types of Grounds***

- Signal Ground
- Common Ground
- Analog Ground
- Digital Ground
- Safety Ground
- Noisy Ground
- Quiet Ground
- Earth Ground
- Hardware Ground
- Single-point Ground
- Multi-point Ground
- Shield Ground

*What about:* **RF Ground?**

Often a ground reference may serve multiple needs, each with a different application.

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## ***Defining "Ground"***

**Power/safety ground**

- Intended (neutral) and unintended (safety ground, generally the green wire)
- 50/60/400 Hz

**Lightning ground**

- A controlled path for lightning to reach the earth through a rod or metallic structure
- Generally a 1 MHz event and up to 100 kAmps per millisecond
- Requires a high quality low ground resistance and inductance

**Circuit/signal ground**

- Provides a return path for intended signal flow and for AC/DC power return; mA to Amps
- Requires a minimum low impedance path
- Generally implemented as a ground plane or grids within a printed circuit board

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# ***Defining "Ground" (continued)***

**EMI ground**

- Provides a controlled path for RF currents; DC to daylight, μA to Amps
- Requires a minimum ground impedance

**ESD ground**

- Provides a controlled path for ESD currents
- 0.7-3 ns rise times, 100-300 MHz, 10-50 Amps

**RF ground**

- Provides an RF return path for flux to return to its source
- Covers the entire frequency spectrum
- Requires minimum impedance for maximum current/flux flow

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# ***Grounding System Topologies***

- **A ground system topology is determined by**
  - Signal characteristics
  - System dimensions
  - System-specific separation and isolation requirements
  - Electrical safety requirements
- **Primary ground system topologies includes**
  - A “floating” system
  - Single-point (“star) ground (SPG)
  - Multi-point ground
  - Hybrid ground

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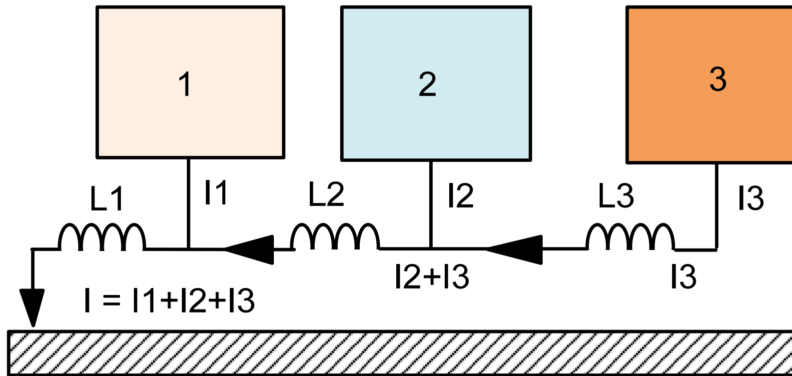
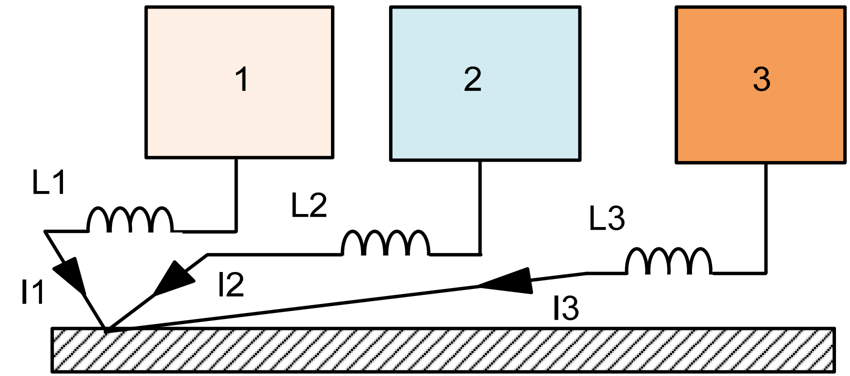
# ***Three Primary Grounding Methodologies***

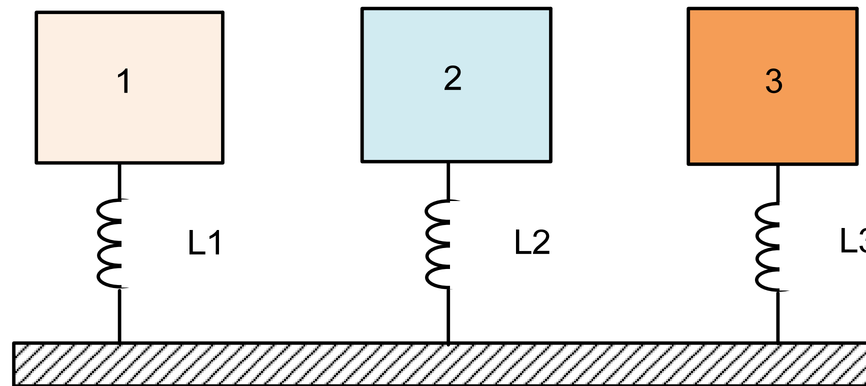
## Single-Point Grounding: Series and Parallel
## Multi-Point




SINGLE-POINT: SERIES CONNECTION




SINGLE-POINT: PARALLEL CONNECTION




MULTI-POINT GROUNDING CONNECTIONS

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**Single-Point: Best for use when signals are below 1 MHz.**

- Most sensitive circuit returns should be connected closest to the final equipotential point.
- Provides for greatest amount of loop currents to flow.
- May be used between 1 and 10 MHz if longest conductor is < $\lambda/20$ of a wavelength of highest frequency generated in the system.
- Divided into two type: series and parallel.

**Multi-Point: Preferred for frequencies above 1 MHz.**

- Minimized loop currents and ground impedance of the planes. A good low inductance ground is necessary for high-frequency digital logic circuits. Ground plane(s) provides a low inductance ground return for RF currents.
- Lead inductance must be kept extremely short.
- Provides for maximum EMI suppression at the PCB level.

**Hybrid: For mixed technology products.**

- A combination of both single-point and multi-point grounding in the same system

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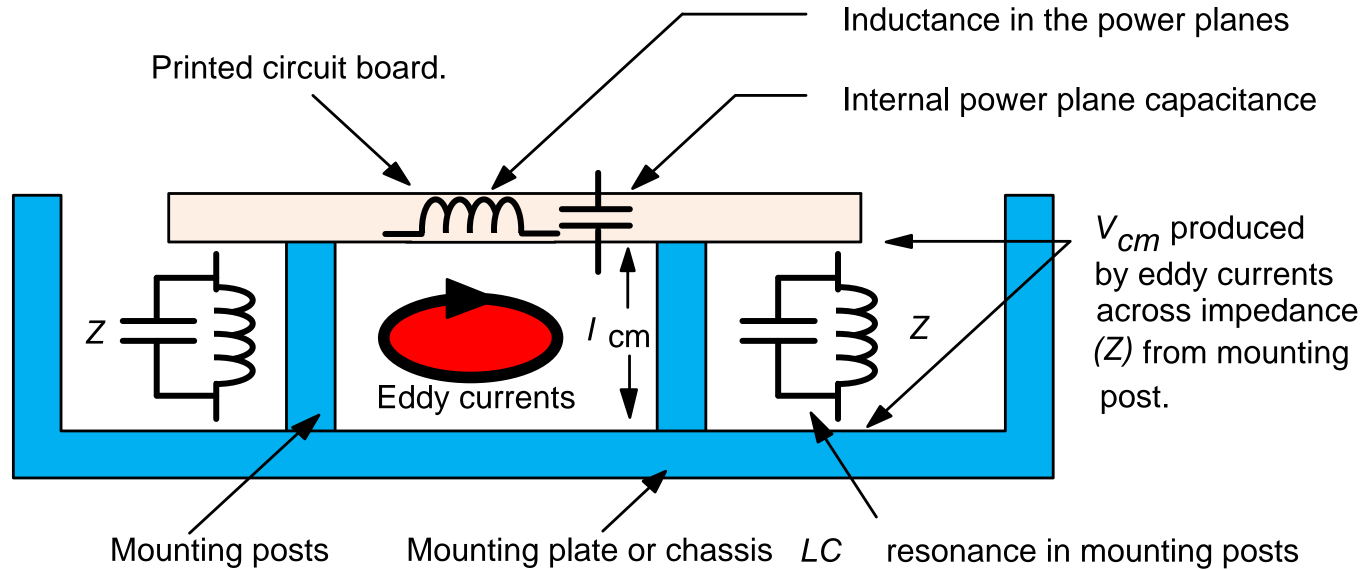
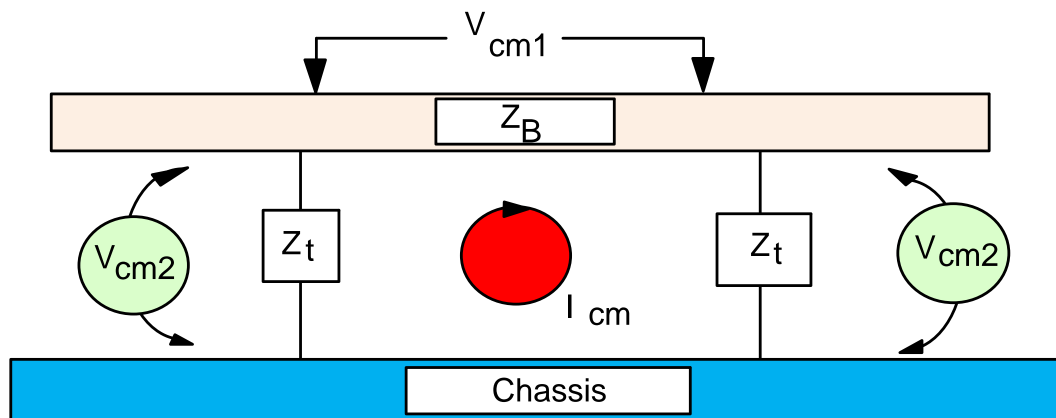
# Resonance in a Multi-Point Ground




**APPLICATION MODEL OF MULTIPOINT GROUNDING**




$V_{cm2}$ is reduced by the mounting posts (ground stitch locations).
Resonance is thus controlled, along with enhanced RF suppression.

**ELECTROMAGNETIC MODEL OF MULTI-POINT GROUNDING**

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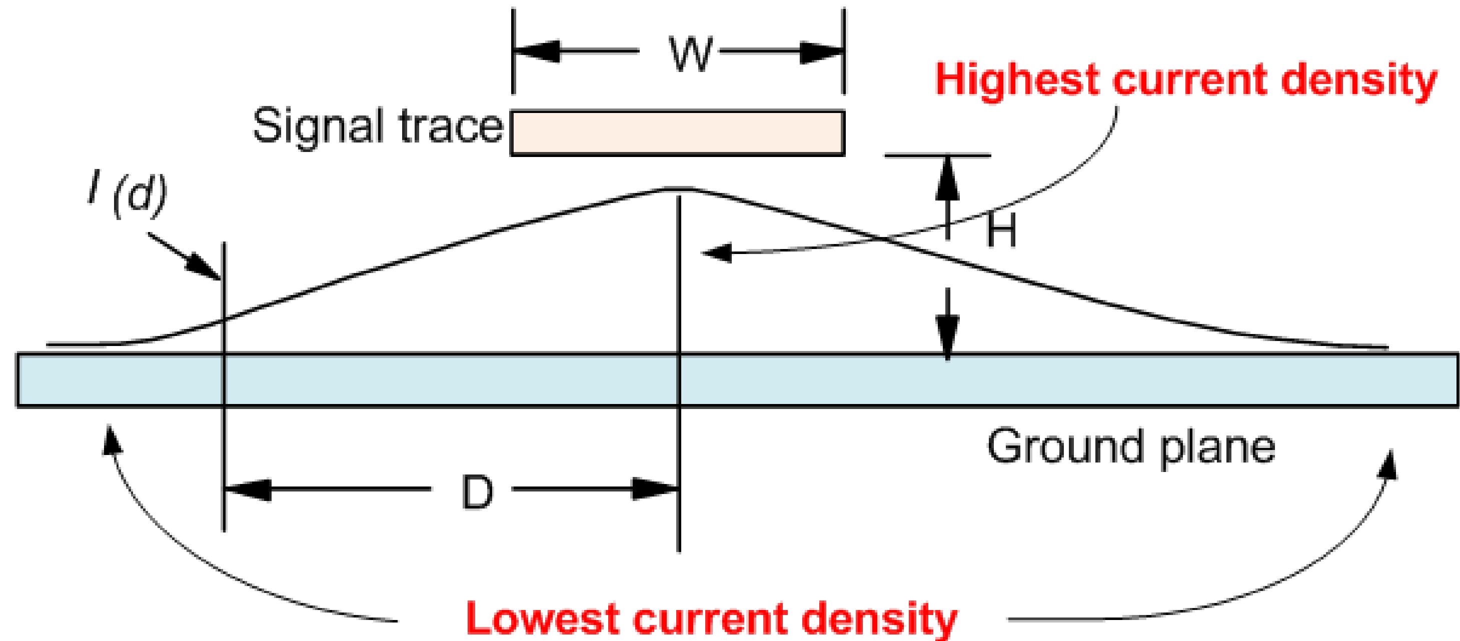
# RF Current Density Distribution




$$I(d) = \frac{Io}{\pi H} \cdot \frac{1}{1 + \left(\frac{D}{H}\right)^2}$$

where $I(d)$ = signal current density, (A/inch or A/cm)
$Io$ = total current (A)
$H$ = height of the trace above the ground plane (in. or cm)
$D$ = perpendicular distance from the center line of the trace (in. or cm)

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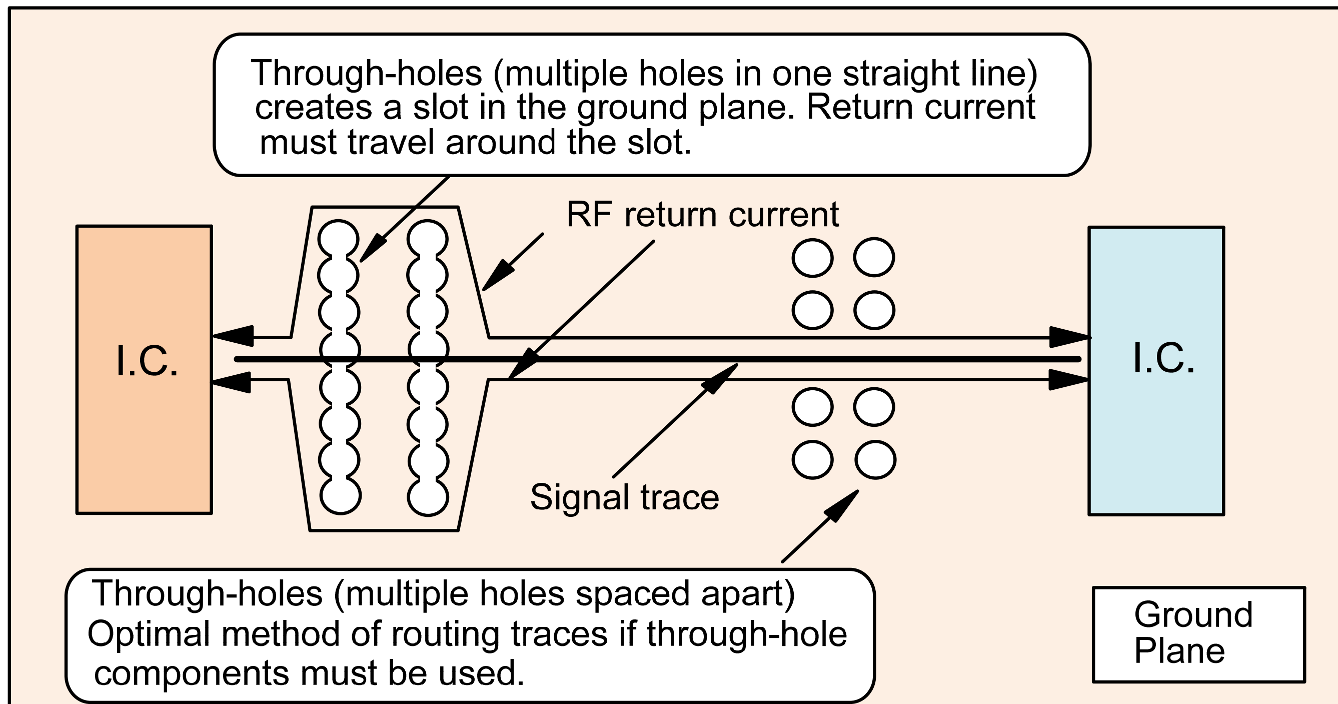
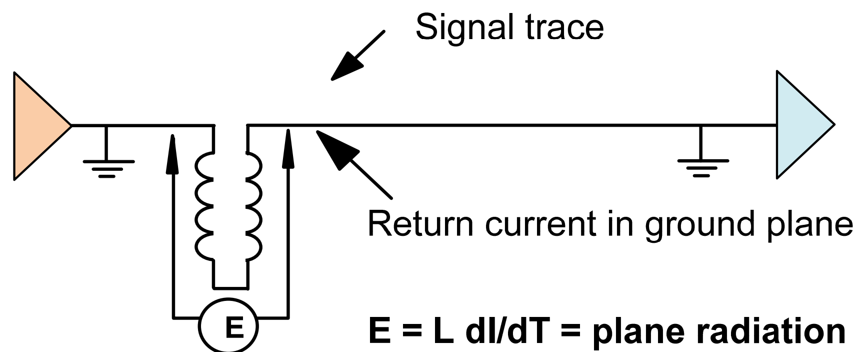
# Ground Slots Created with Through-Hole Components




Equivalent circuit showing inductance in the return path. This inductance is approximately 1 nH/cm.

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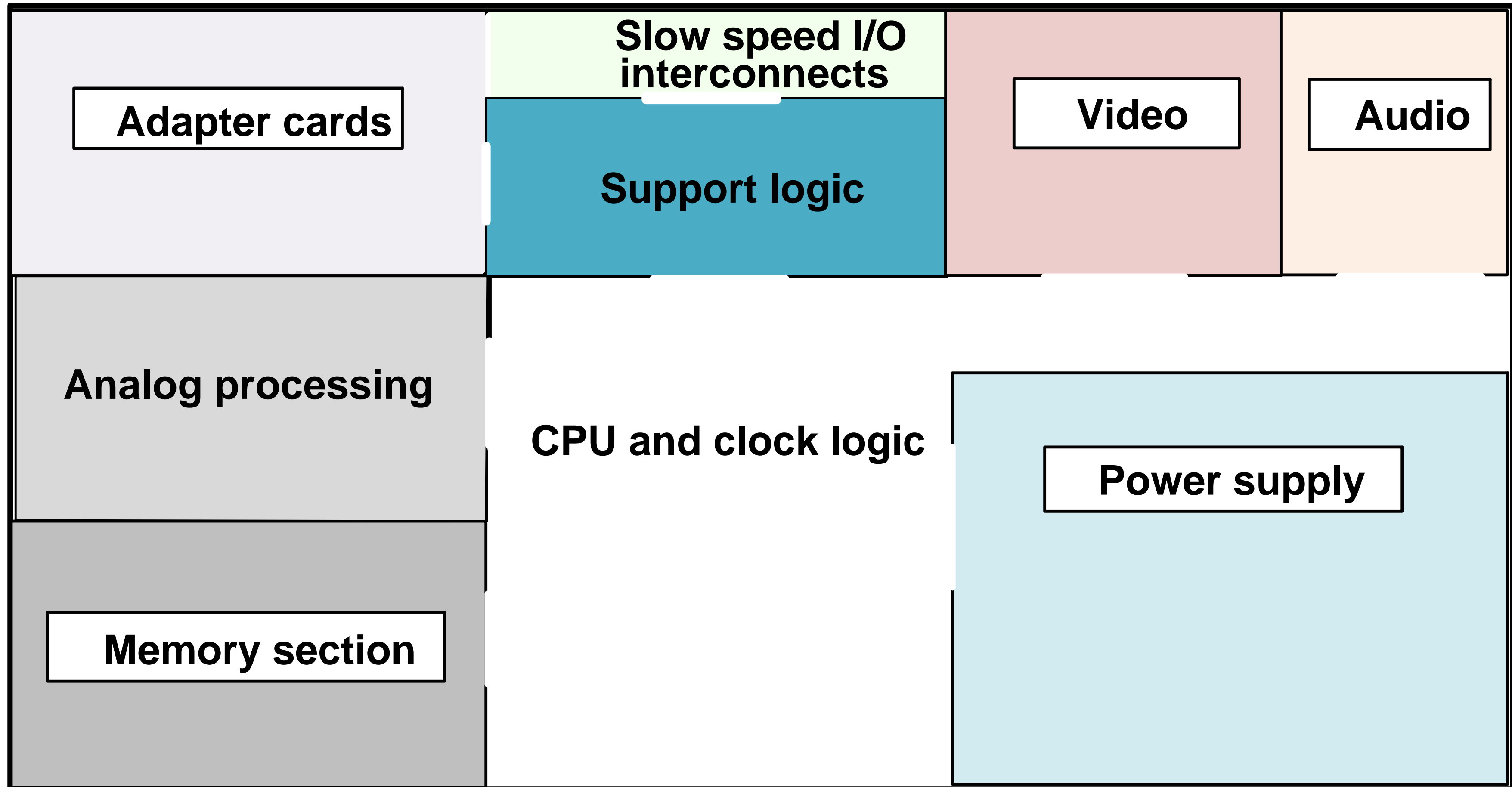
# ***Functional Partitioning***

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# *Bypassing and Decoupling (Power Distribution Networks)*

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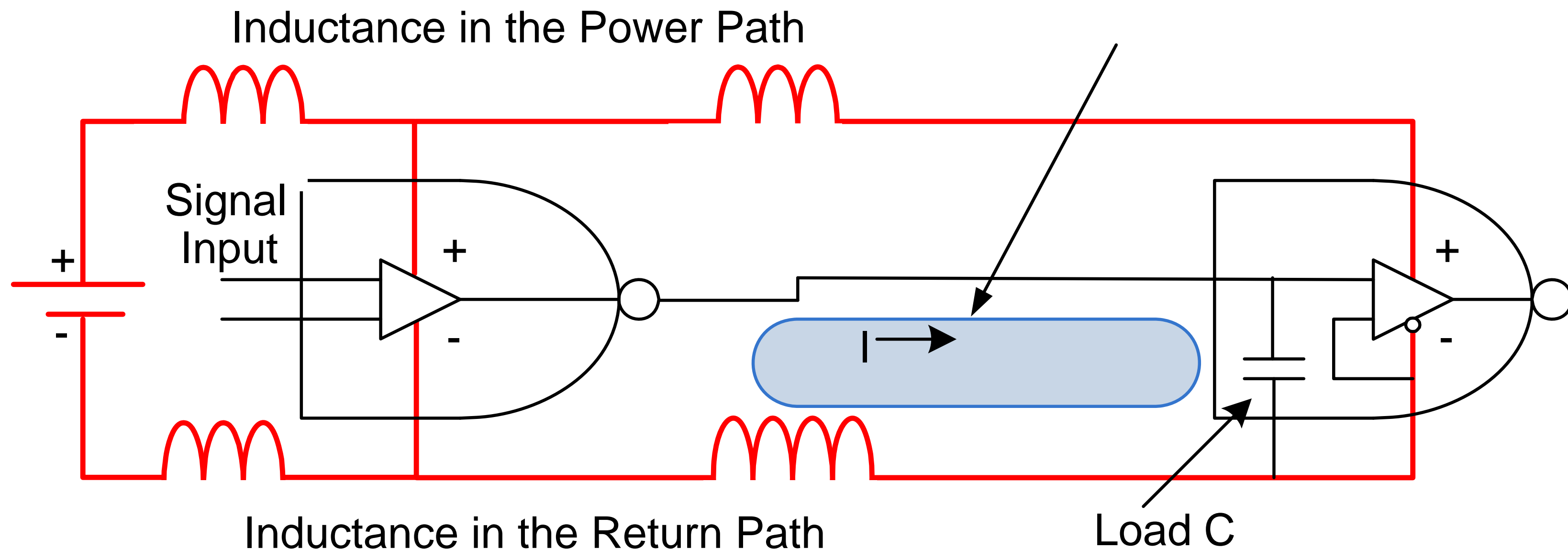
# *The Need for Optimal Power Distribution*

- Provides a stable voltage reference between components to ensure functional operation
- Distribute optimal power to all logic devices to minimize planar bounce

## Key items of concern

**Use low impedance connections between logic gates:**

- The impedance between power pins on gates should be just as low as the impedance between the return pins on the same device
- A low impedance path must always be provided between power and return

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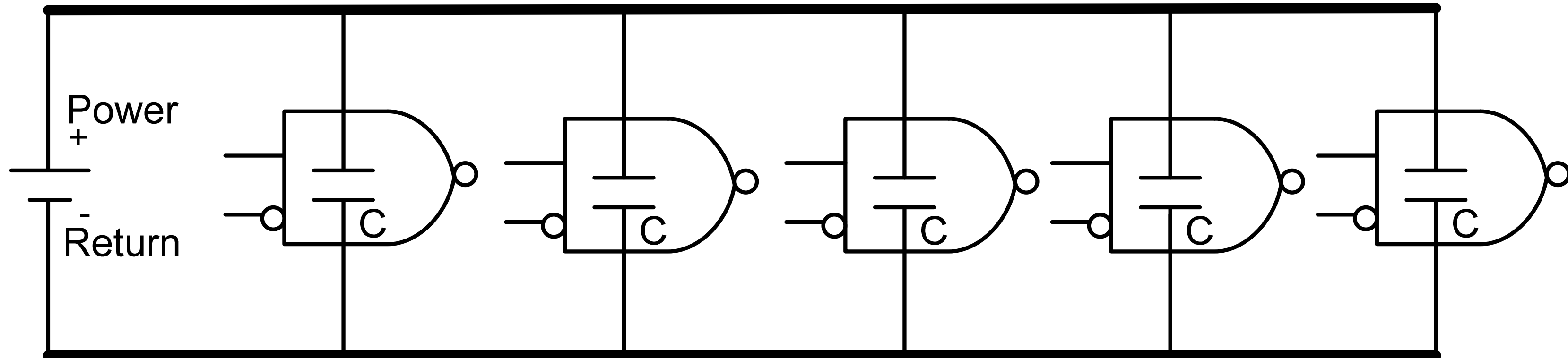
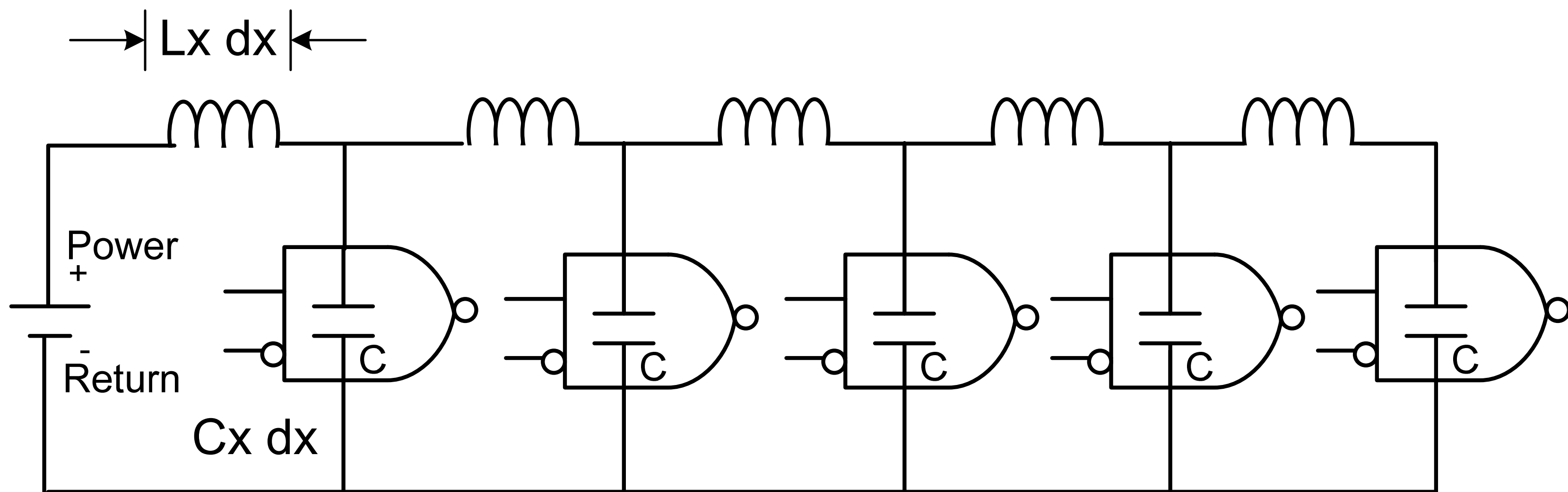
# ***Power Distribution Networks as Transmission Lines***

Power distribution networks can be represented as a two conductor transmission line with a defined characteristic impedance and propagation delay.




**Ideal Power Distribution Network – Multiple Loads**




**Real-Life Power Distribution Network – Multiple Loads**

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## ***Primary Requirements for Enhanced Power Distribution***

The amplitude of power supply transients are directly proportional to the characteristic impedance of the power distribution system, $Z_0$:

**To reduce $Z_0$**

- Reduce inductance
- Increase capacitance

$$Z_o = \sqrt{\frac{L_o}{C_o}} = \frac{V_{(x)}}{I_{(x)}}$$

**Both are achieved by**

- Reduction of loop area between conductors (less inductance)
- Placing conductors as close together as possible (greater capacitance)
- Increase of conductors' width (less inductance and greater capacitance, with respect to another conductor)

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# ***Defining Capacitor Usage***

**Capacitors are used for one of three primary functions.**

**Bulk** Used to maintain constant DC voltage and current levels on a global basis due to IR drops within the power distribution network, and to recharge the distribution network (i.e., planes) cause by *dI/dt* consumption from components (typically 1-100 µF).

**Bypassing** Diverts or steers RF currents from one location to another. Shunts unwanted common-mode RF currents from components or cables from entering susceptible areas in addition to providing other functions of filtering (bandwidth limited).

**Decoupling** Provides a localized source of DC power, and are particularly useful in reducing peak current surges propagated across the board. Prevents RF currents from being injected into the power distribution network during digital component edge transitions.

- Switching transient capacitance (0.01 µF) – Used to supply short-term energy demands of the silicon during switching states.
- Line charging capacitance (0.1 µF) – Used to charge capacitive transmission lines as well as supplying current necessary for the driver.

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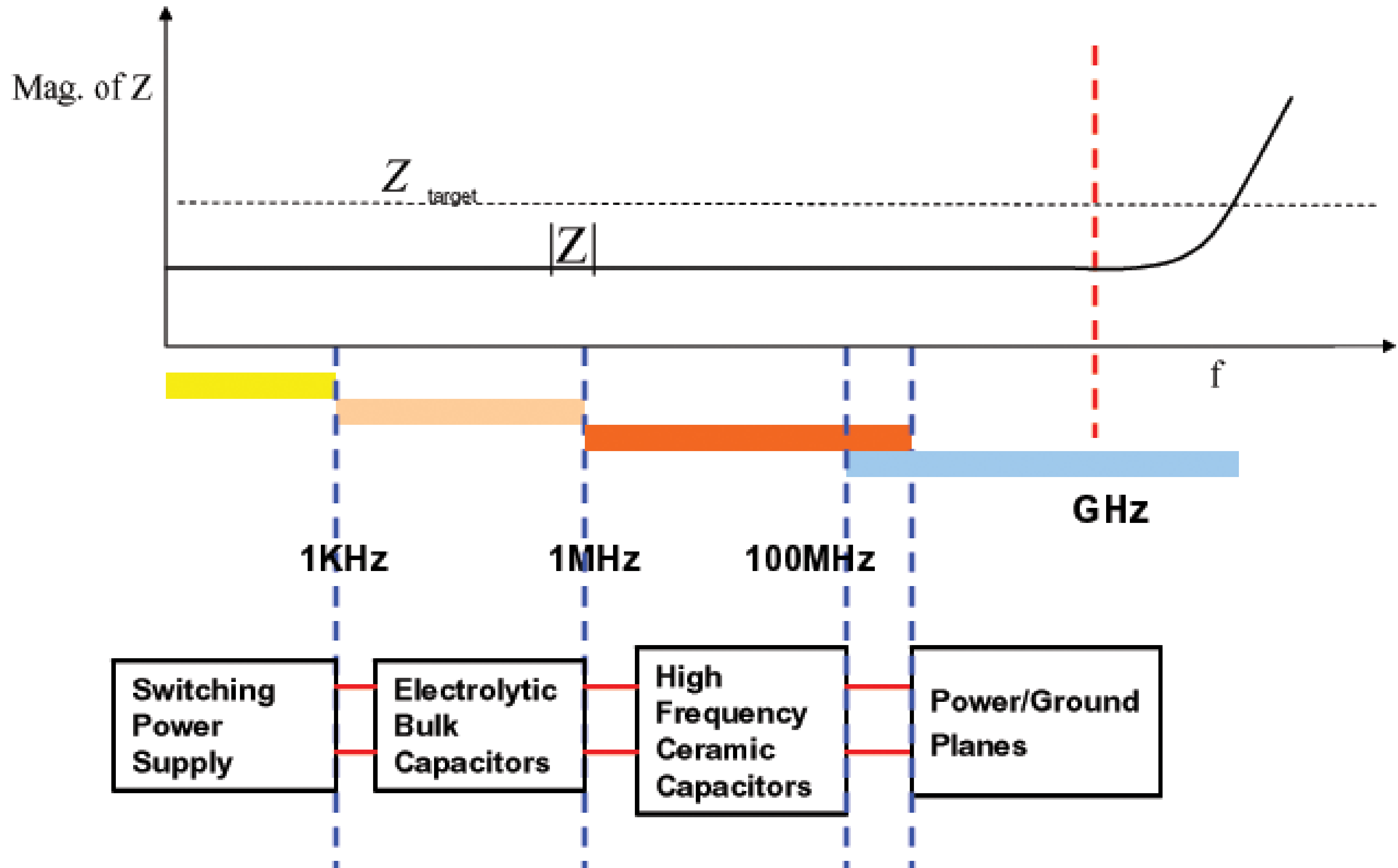
# Effective Range of Decoupling Systems and Target Impedance




(Artwork provided courtesy – Ansoft Corporation)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## ***Calculating Power and Return Plane Capacitance***

Capacitance of the power and ground planes is defined by:

$$C_{pp} = k\frac{\varepsilon_r A}{D}$$

where

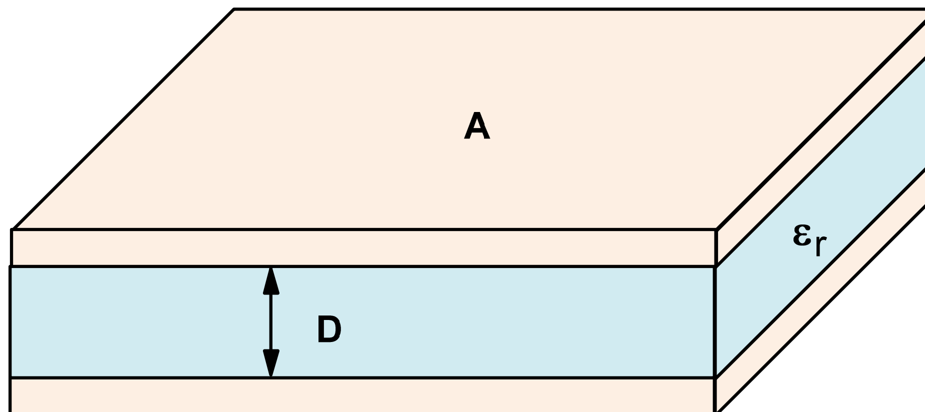
$C_{pp}$ = capacitance of parallel plates (pF)

$\varepsilon_r$ = *dielectric constant of the board material*

*A = area between the parallel plates (square inches or cm)*

*D = distance spacing between the plates (inches or cm)*

*k = conversion constant (0.2249 for inches, 0.884 for cm)*

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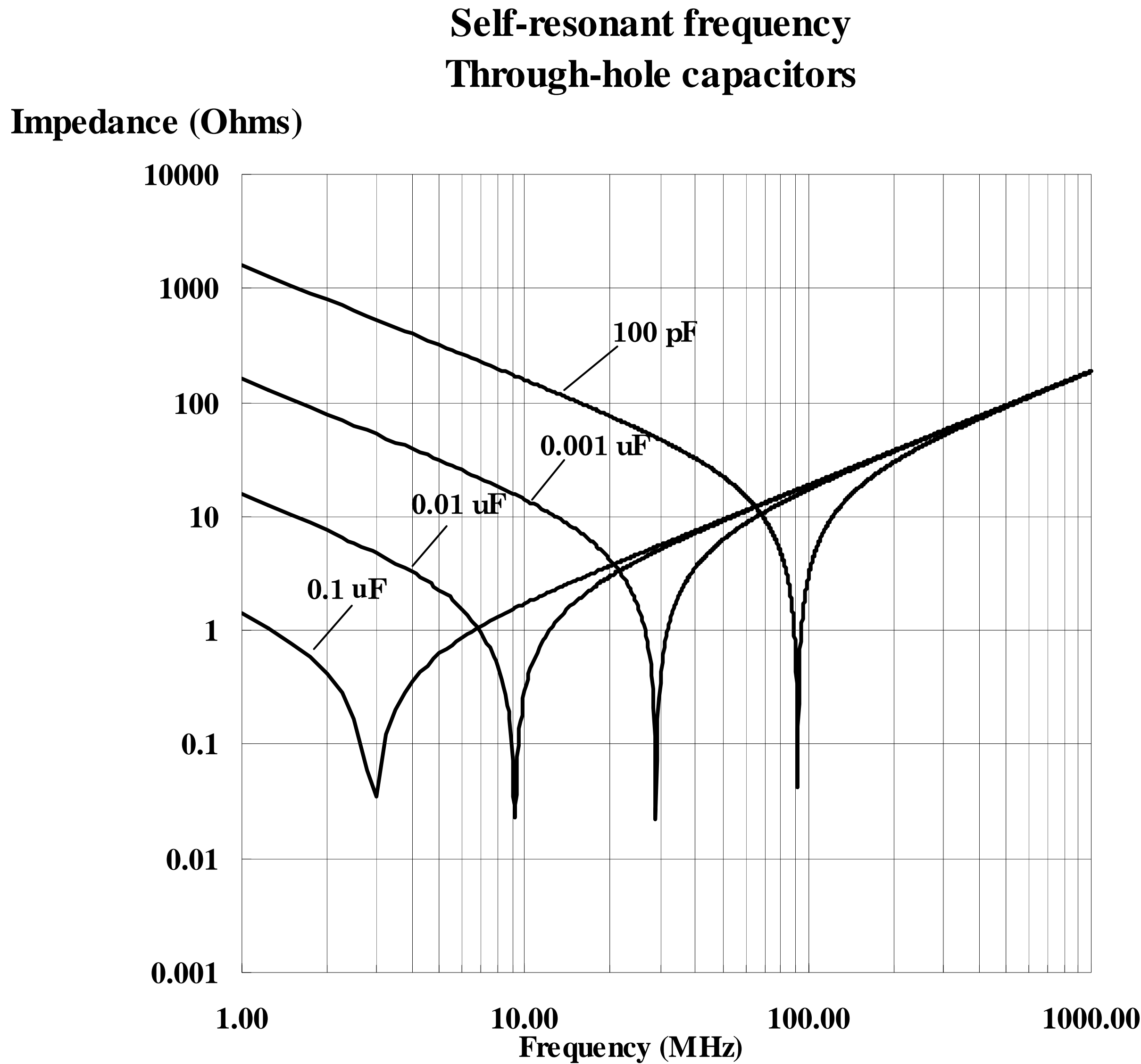
# Capacitors and Resonance




## 1/4 inch or 0.64 cm leads – 15 nH

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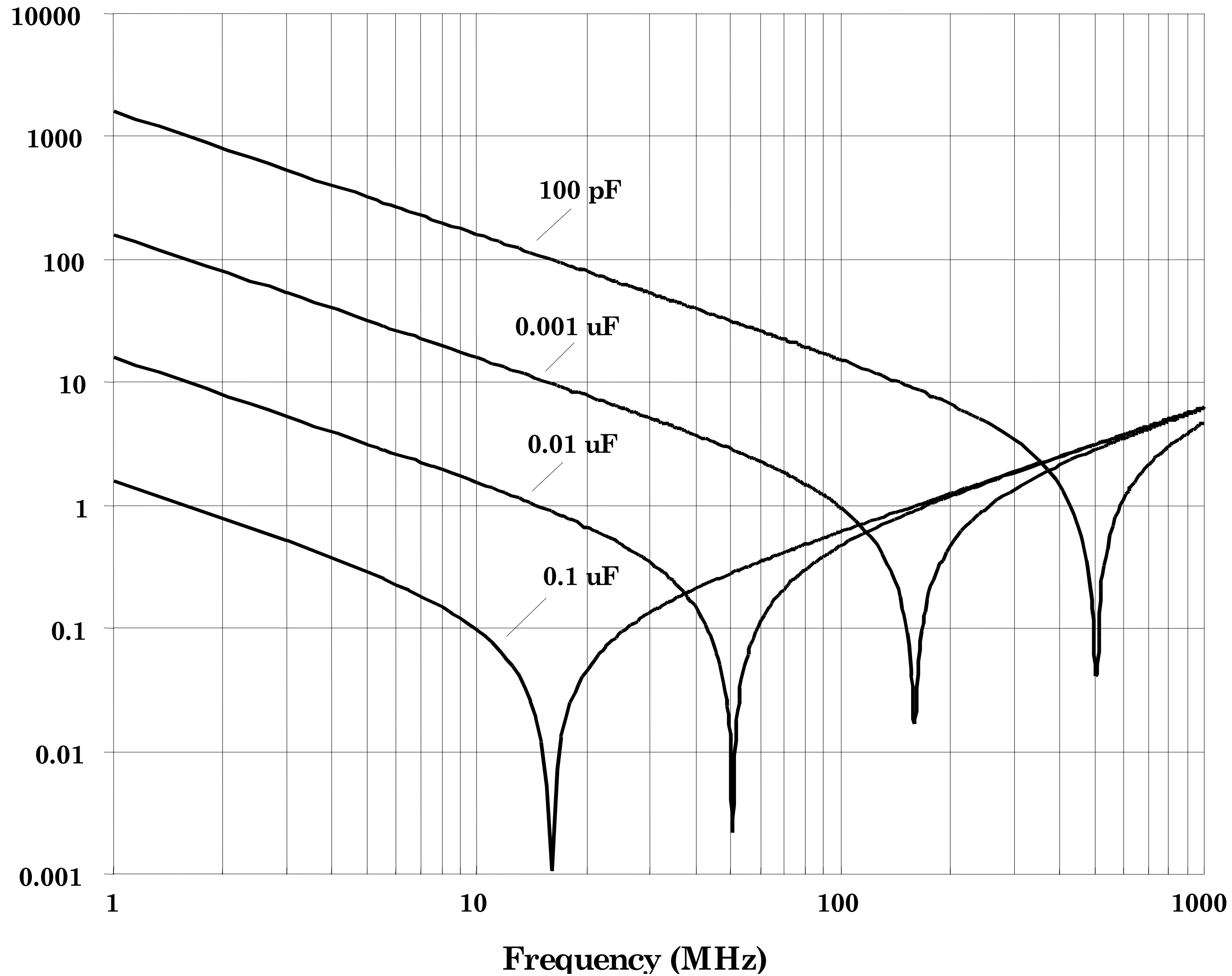


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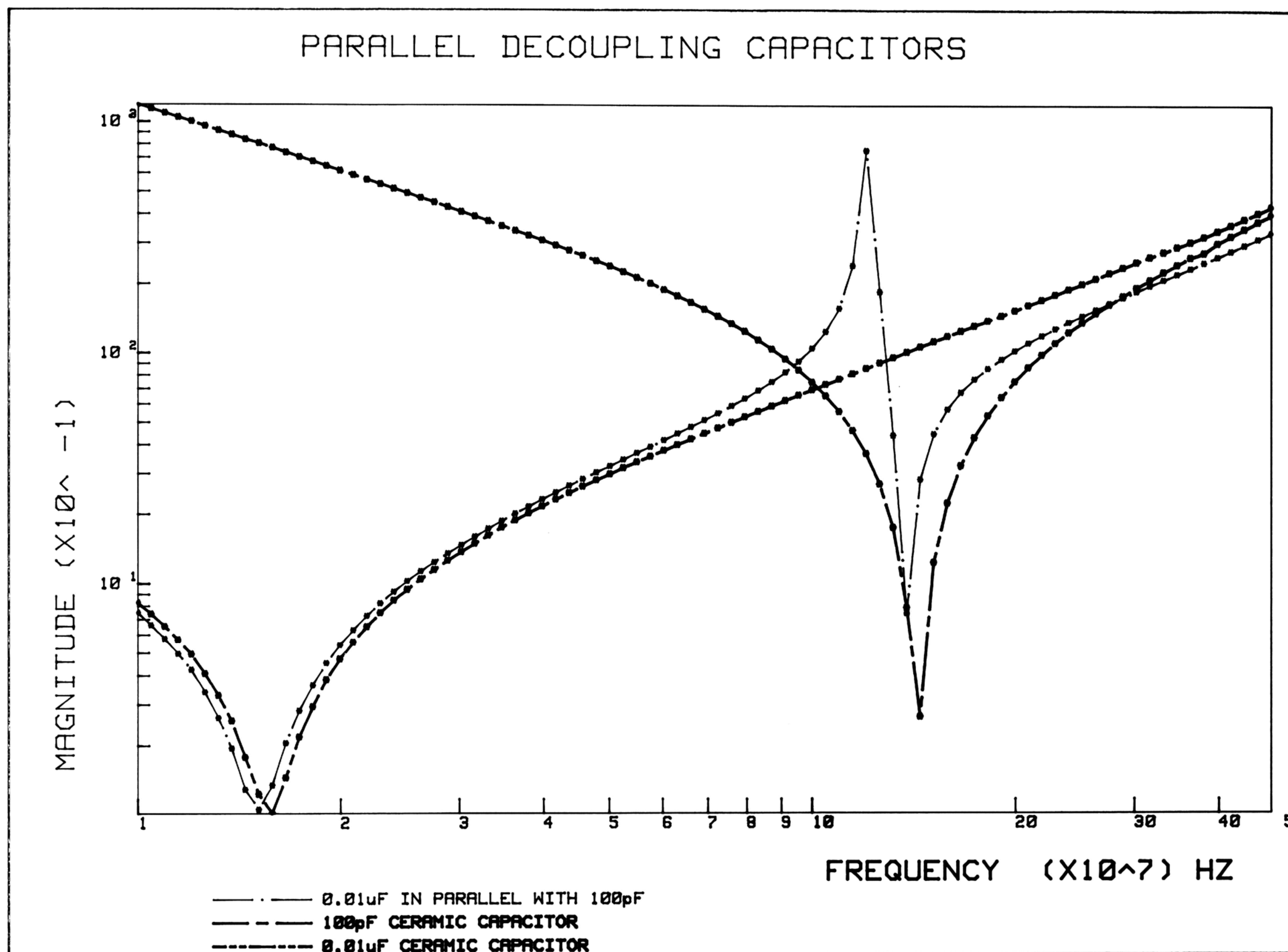
# ***Effects of Capacitors in Parallel – Different Values***

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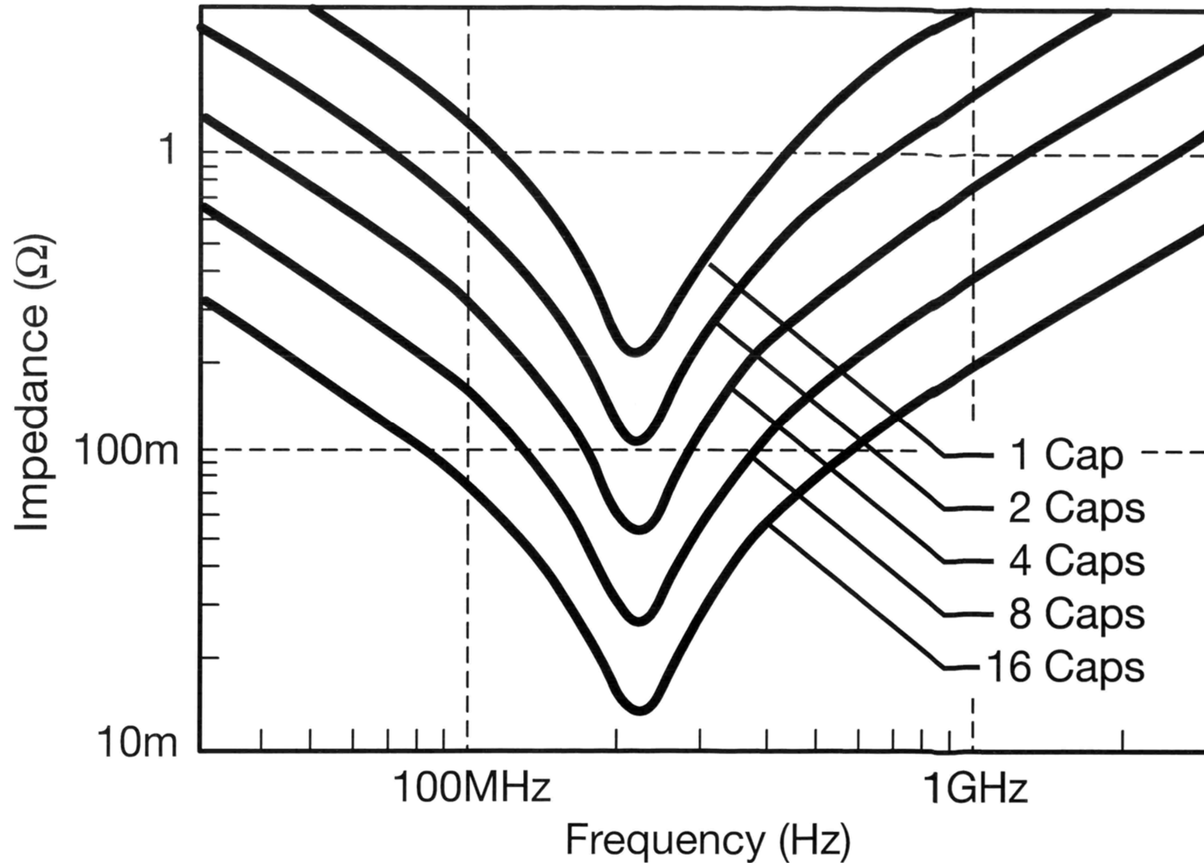
# Effects of Capacitors in Parallel – Same Capacitor Values




How to calculate number of capacitors with the same capacitive value in parallel:

(Plot provided courtesy AVX Corp.)

$$C_{total} = n * C$$

$$L_{otal} = \frac{L}{n}$$

$$ESR_{total} = \frac{ESR}{n}$$

$$|Z| = \sqrt{\left(\frac{ESR}{n}\right)^2 + \left(\frac{\omega ESL}{n} - \frac{1}{\omega nC}\right)^2}$$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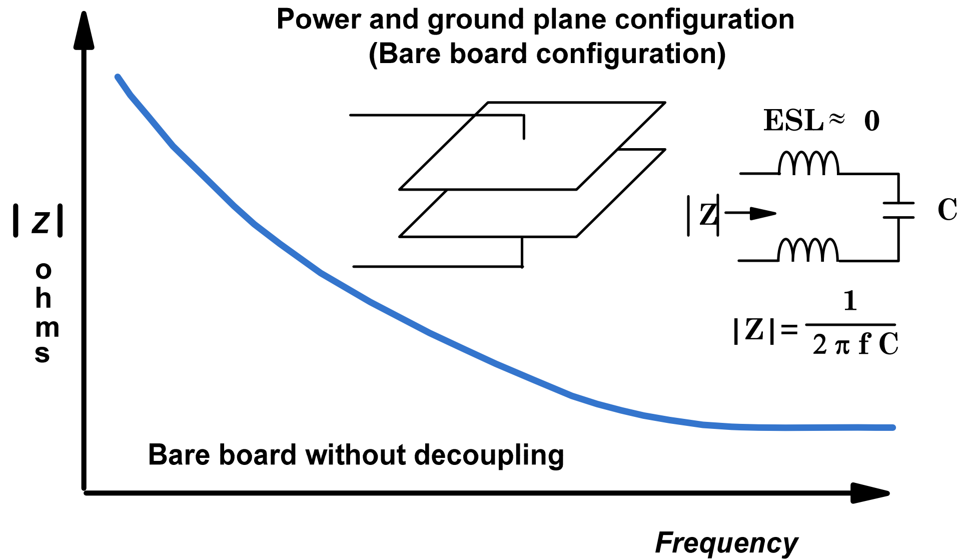
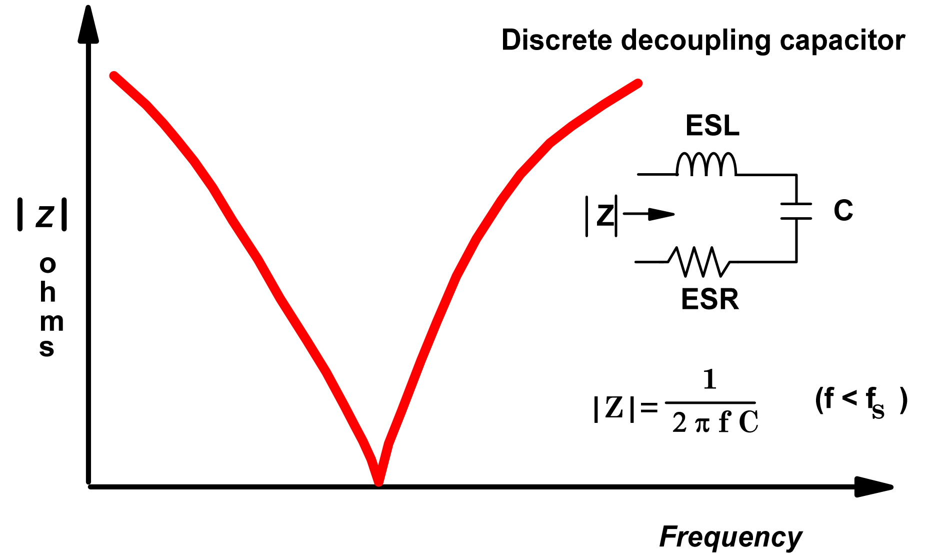
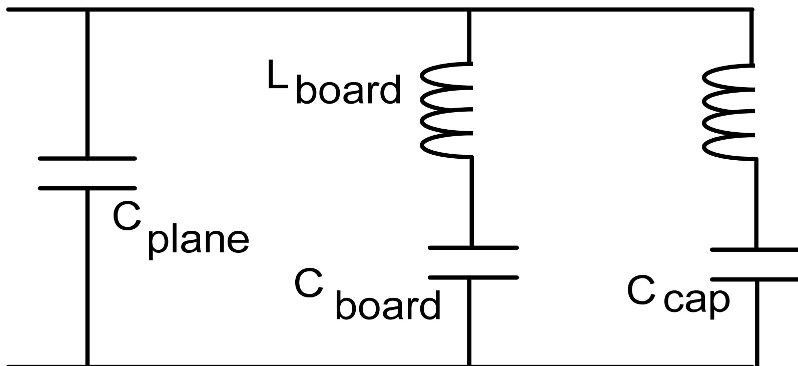
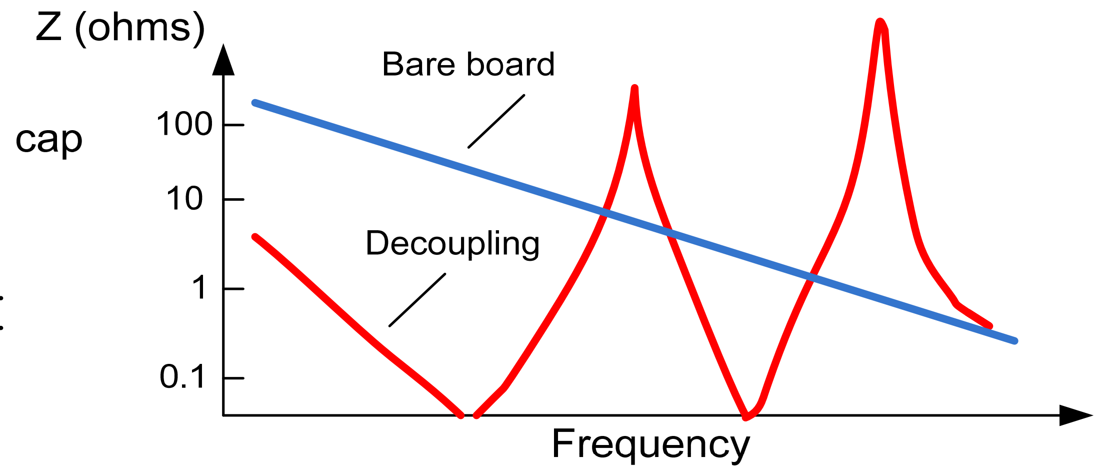
# Power and Ground Plane Capacitance





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## *Conflicting Rules for PCB Decoupling*

**Use small-valued capacitors for high-frequency decoupling**

**Use 0.01 μF for local decoupling**

**Locate capacitors near the power pins of active devices**

**Use capacitors with a low ESR!**

**Avoid capacitors with a low ESR**

**Locate capacitors near the ground pins of active devices**

**Locate of the decoupling capacitors is not relevant**

**Use 0.001 μF for local decoupling**

**Never put traces on decoupling capacitors**

**Use the largest valued capacitors you can find in a given package size**

**Local decouping capacitors should have a range of values from 100 pf to 1 μF**

List created by Todd Hubing

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# *Interconnects and I/O*

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# ***Partitioning***

## Functional Subsystems

A group of components along with their respective support circuitry performing a common function.

## Quiet Areas

Sections physically isolated from other functional areas to prevents noise sources from corrupting susceptible circuits in the quiet zone.

## Internal Radiated Noise Coupling

Radiated RF coupling may occur between different functional subsections. To prevent this coupling, a *fence* or shield barrier may be required. A fence is a metal barrier secured to the ground plane(s) at intervals appropriate for the highest frequencies anticipated (at $\lambda/20$ wavelength intervals) and tall enough in height to prevent direct line RF radiated field coupling.

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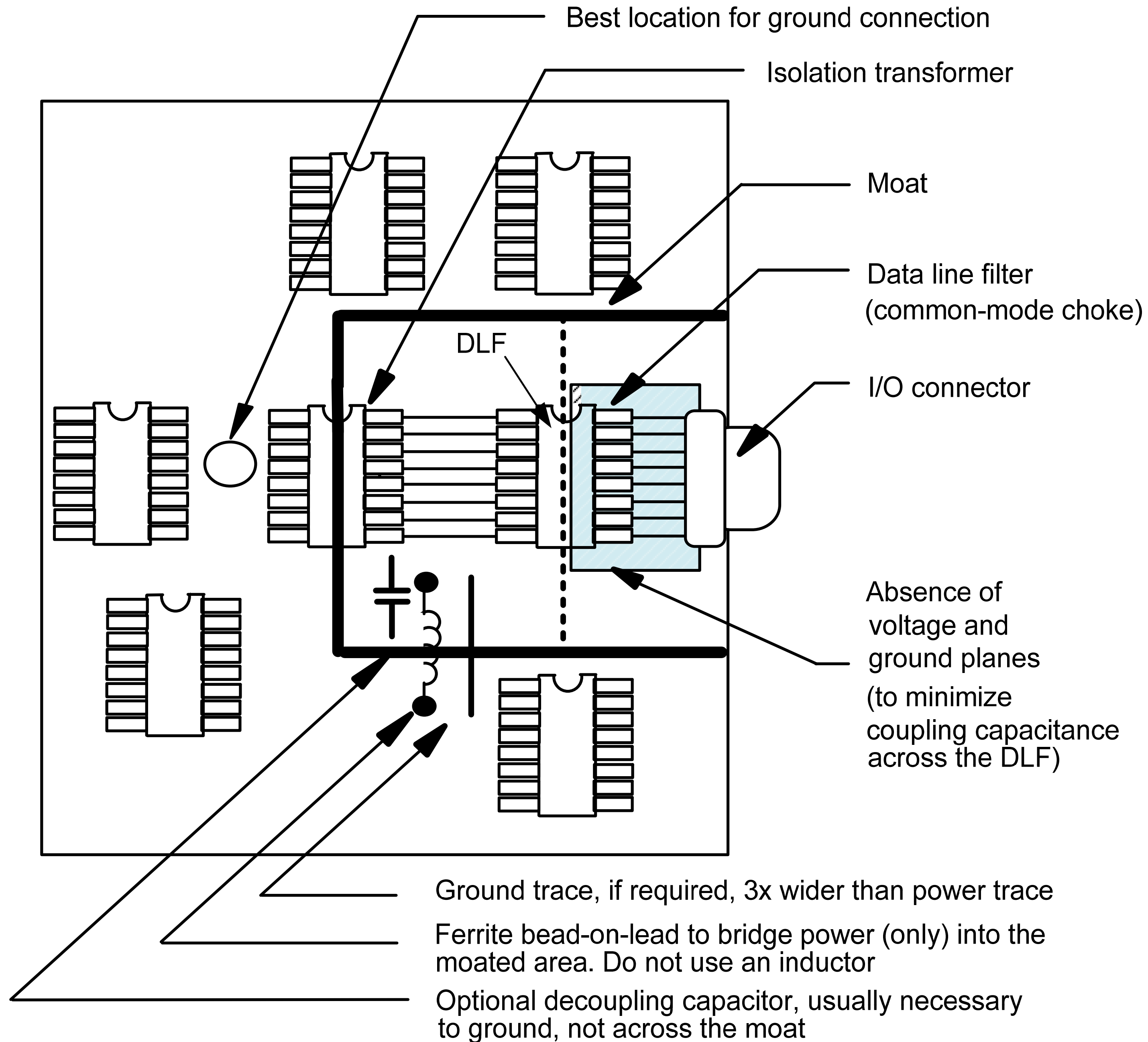
# Isolation (Moating)

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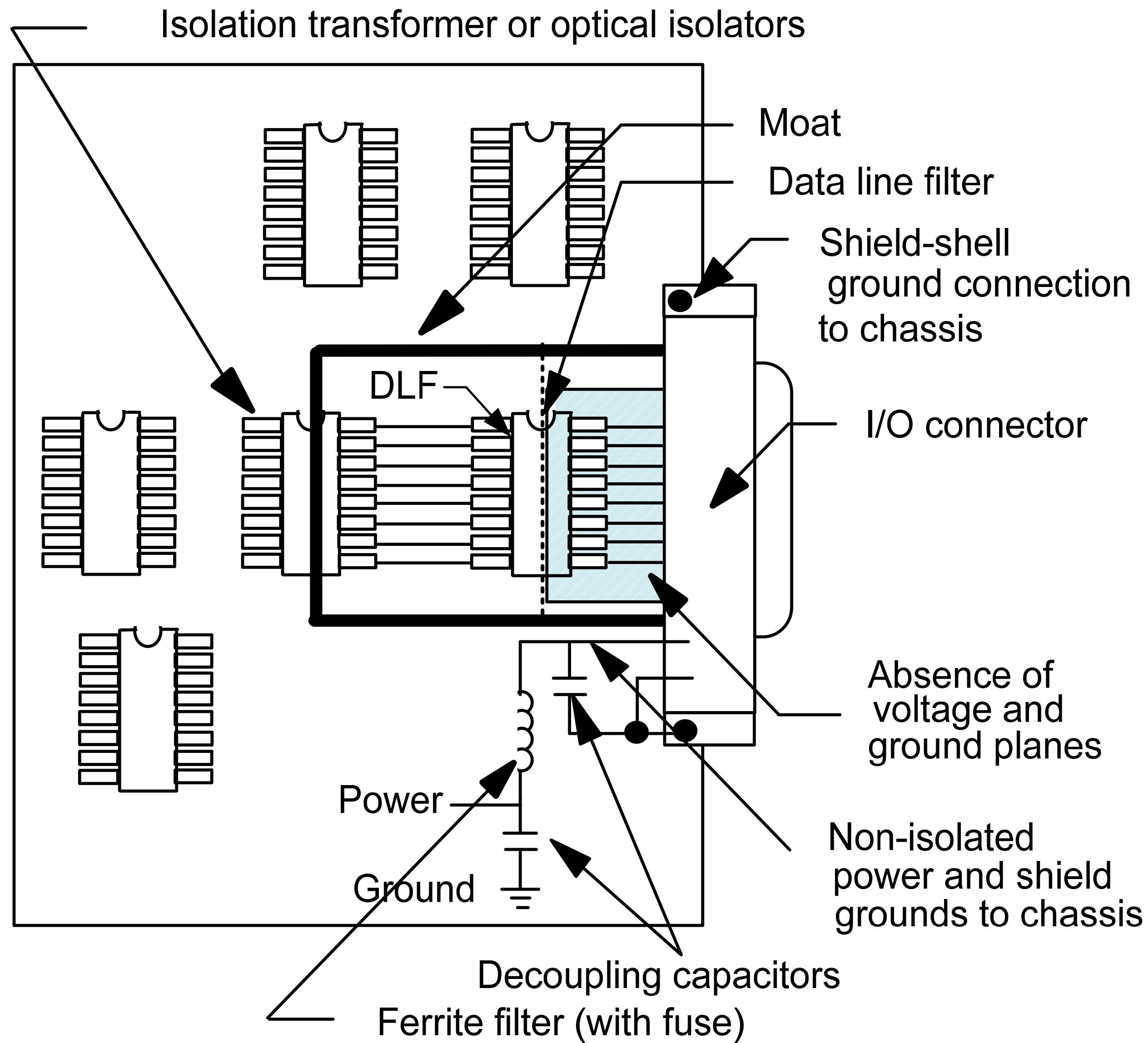


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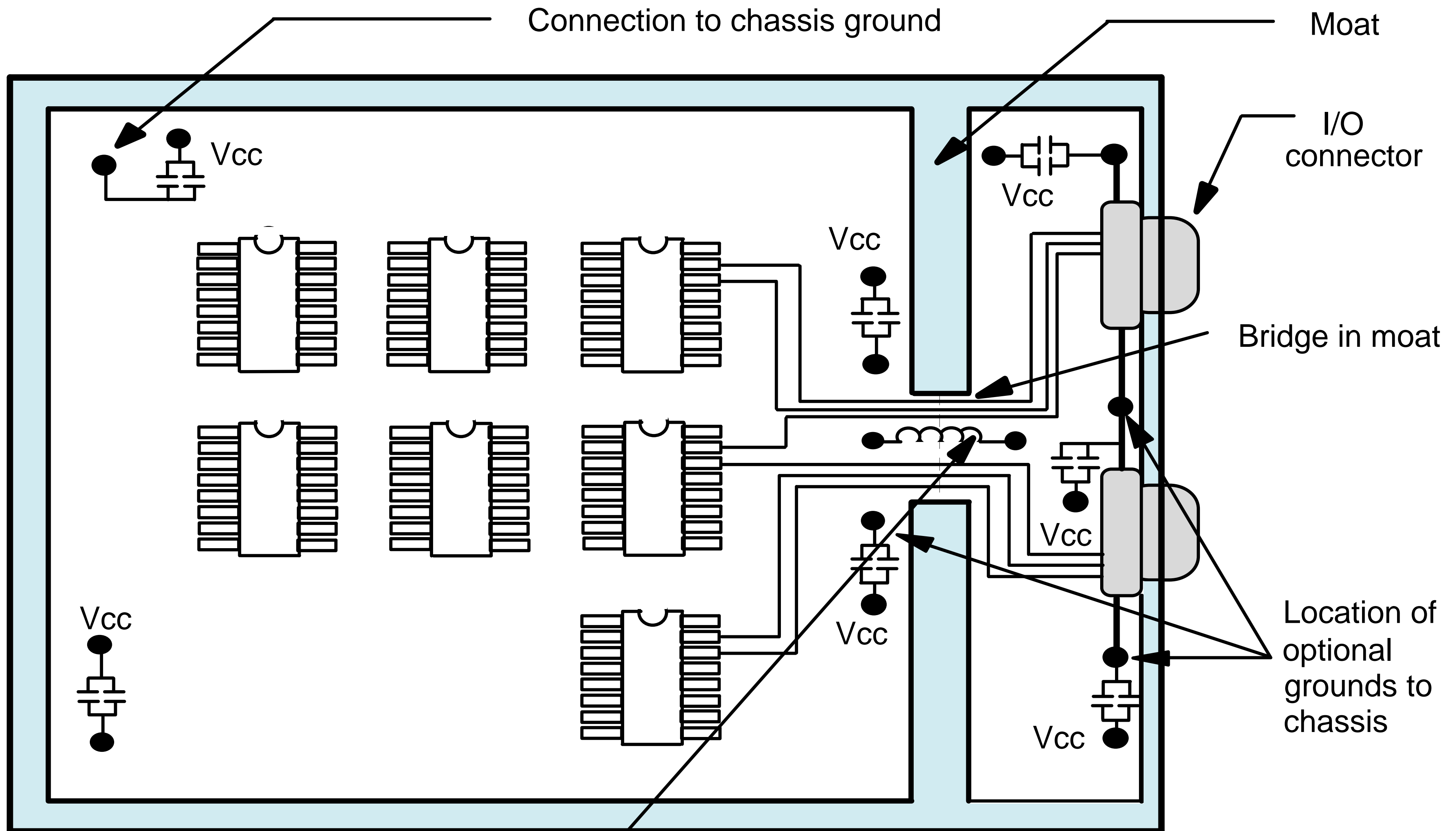
# Bridging




Ferrite bead-on-lead for optional power, if required, over a separate moat for power plane. (dotted line).

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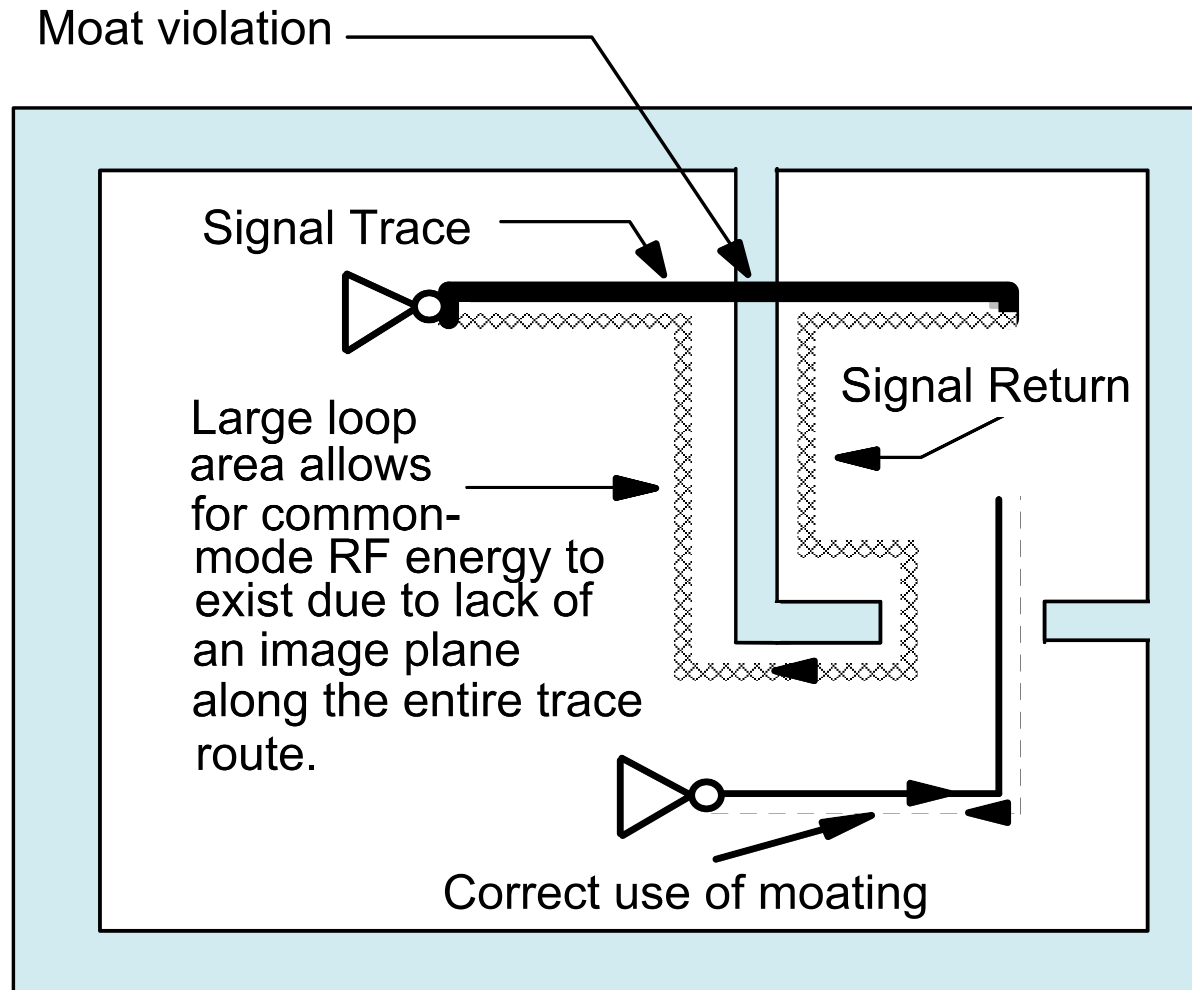
# *Image Plane or Moat Violation*

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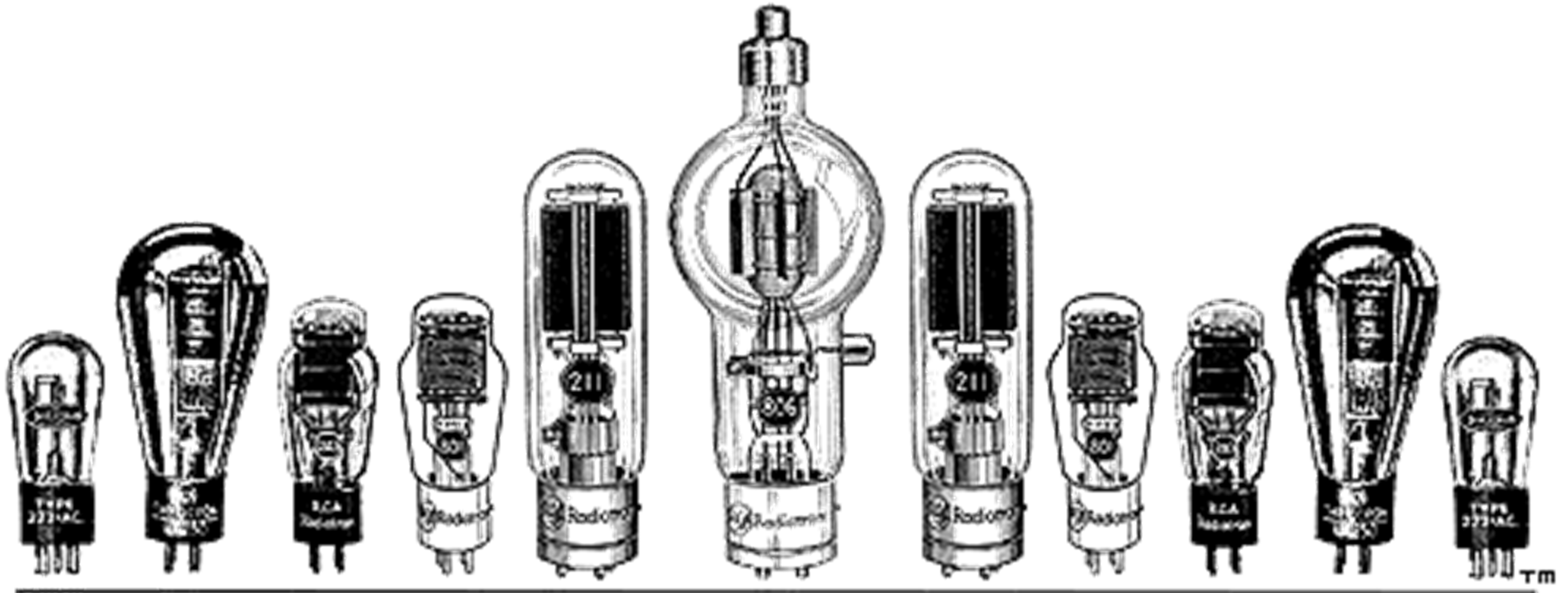
# Solution to All EMC Problems

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